Clase 1:

IB 2014

Adaptado de:

Digital Integrated Circuits
A Design Perspective

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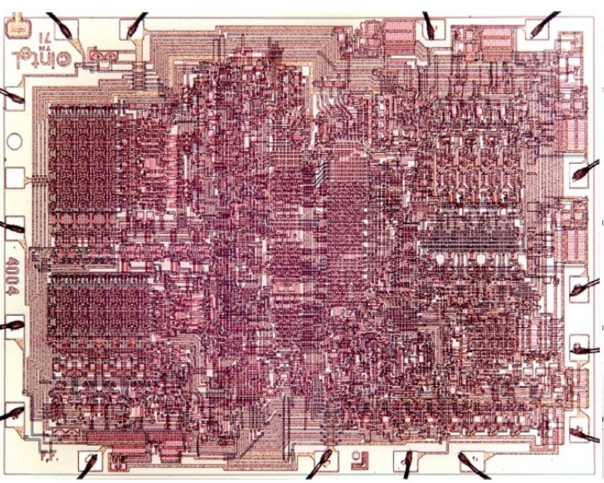
¿Por qué estudiar MOS y CMOS?

Dispositivos MOS y circuitos CMOS:

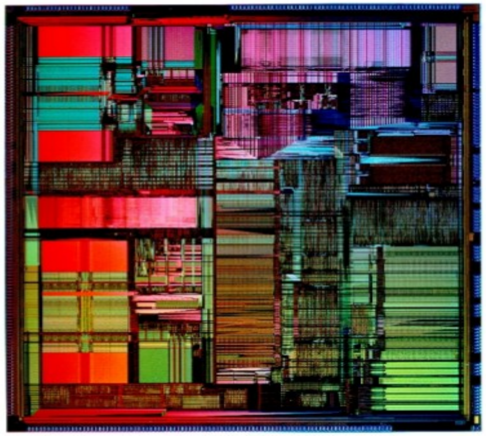
• Los transistores MOS (MOSFETs) son la cosa más fabricada por la humanidad, ~10^{19} trans por año (~2^{63})

• Toda la electrónica digital está basada en transistores MOS, en lógica complementaria (CMOS). Buena parte de la analógica también.

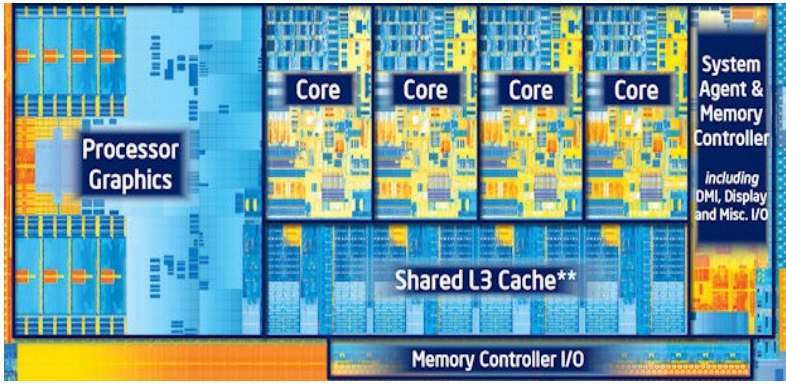
2^{56}	2^{57}	2^{58}	2^{59}	2^{60}	2^{61}	2^{62}	2^{63}
2^{48}	2^{49}	2^{50}	2^{51}	2^{52}	2^{53}	2^{54}	2^{55}
2^{40}	2^{41}	2^{42}	2^{43}	2^{44}	2^{45}	2^{46}	2^{47}
2^{32}	2^{33}	2^{34}	2^{35}	2^{36}	2^{37}	2^{38}	2^{39}
2^{24}	2^{25}	2^{26}	2^{27}	2^{28}	2^{29}	2^{30}	2^{31}
2^{16}	2^{17}	2^{18}	2^{19}	2^{20}	2^{21}	2^{22}	2^{23}
2^{8}	2^{9}	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}
2^{0}	2^{1}	2^{2}	2^{3}	2^{4}	2^{5}	2^{6}	2^{7}



Primer procesador, INTEL 4004 (4 bits), 1971, 3.500 transistores, 740kHz, 10um, 630mW, 12mm2

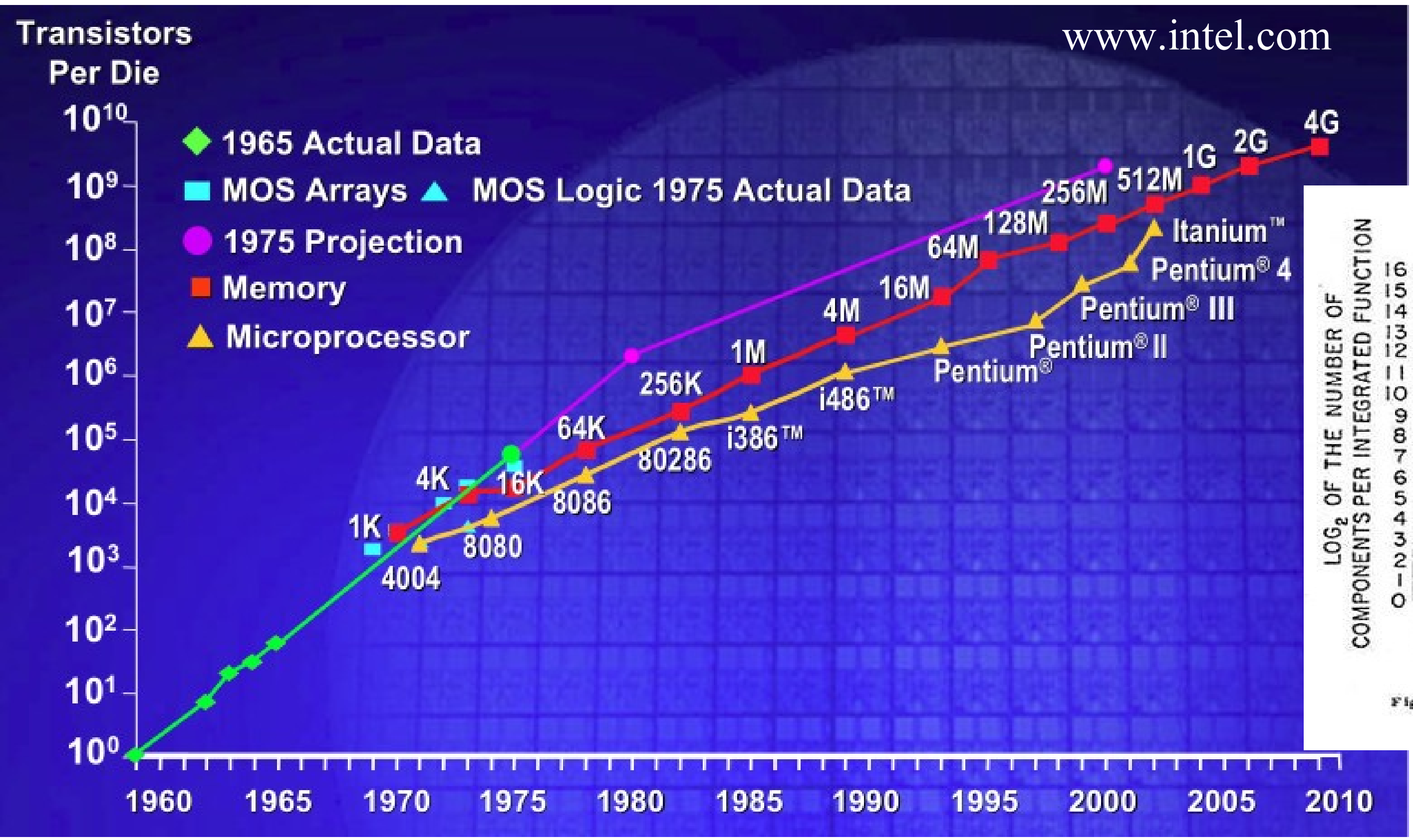


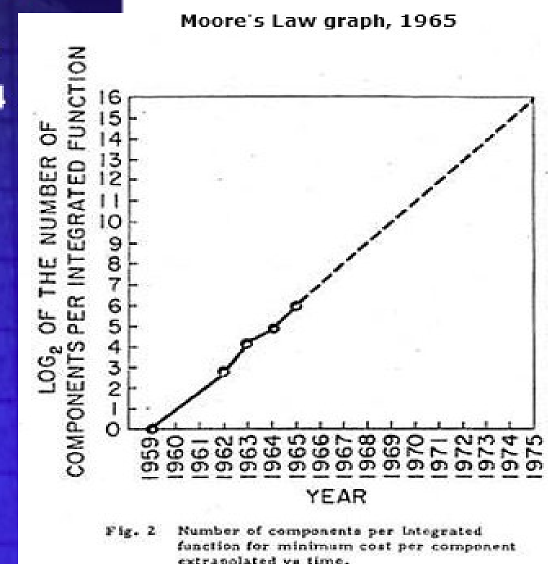
Intel Pentium 1993, 3.100.000 transistores, **0,5um**, 100MHz, 290mm^2 .



Intel Core i7 2013, 10^9 transistores, 22nm, 2-3GHz, 100-200mm^2 .

Ley de Moore





Moore, 1965
(co-fundador de intel)

”Cada 18 meses se duplica el número de transistores en un circuito integrado.”

Luego se reformuló, se duplica el número de dispositivos cada dos años

Dispositivos en un proceso CMOS comercial.

Schematic Cross Sections

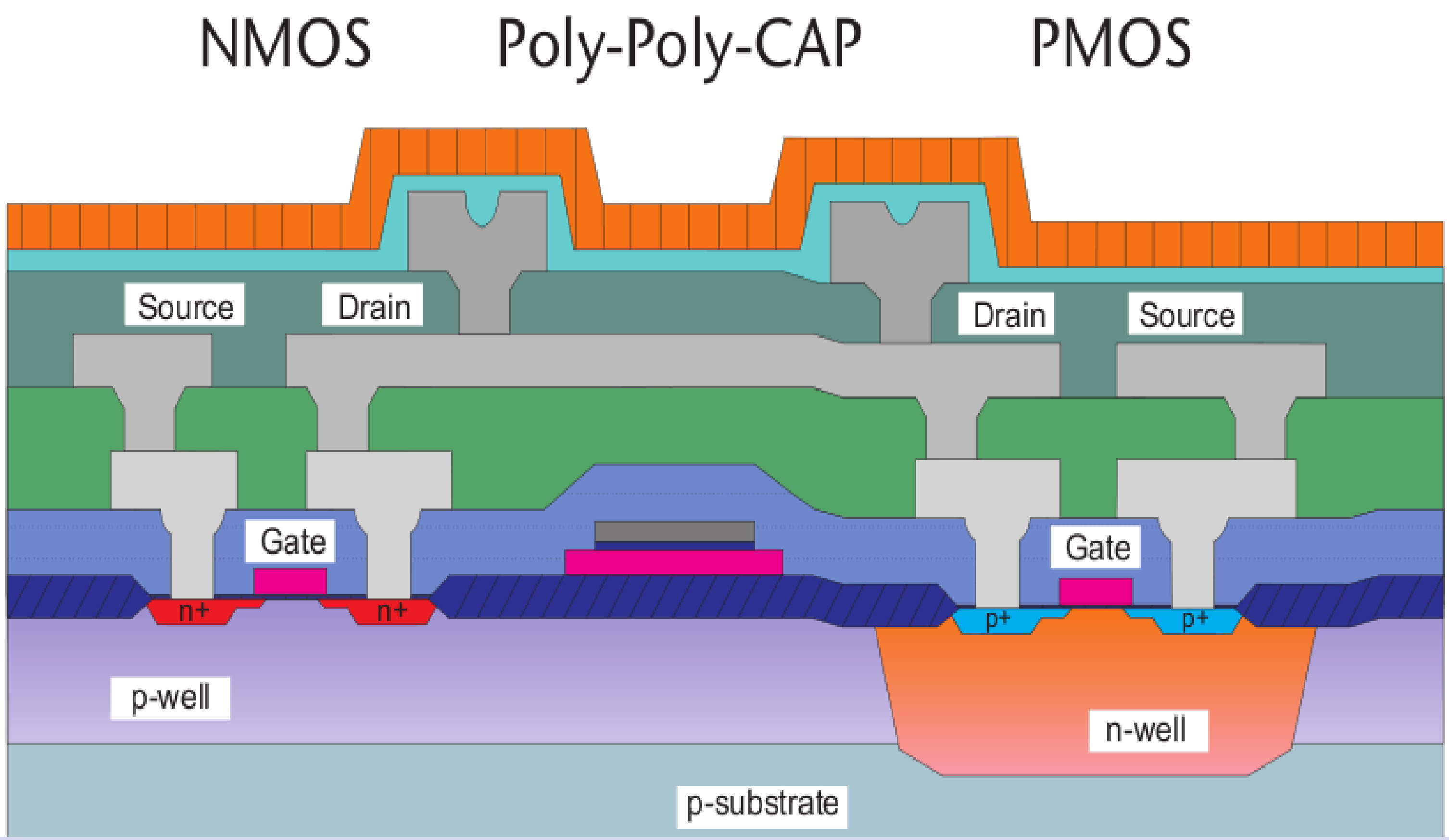
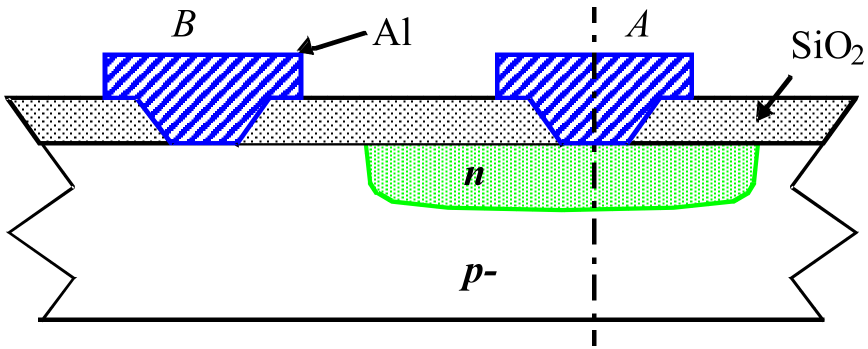
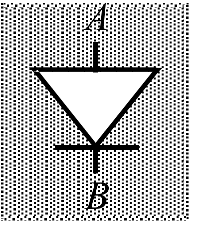


Figure 1: 5V devices

Diodo en procesos CMOS



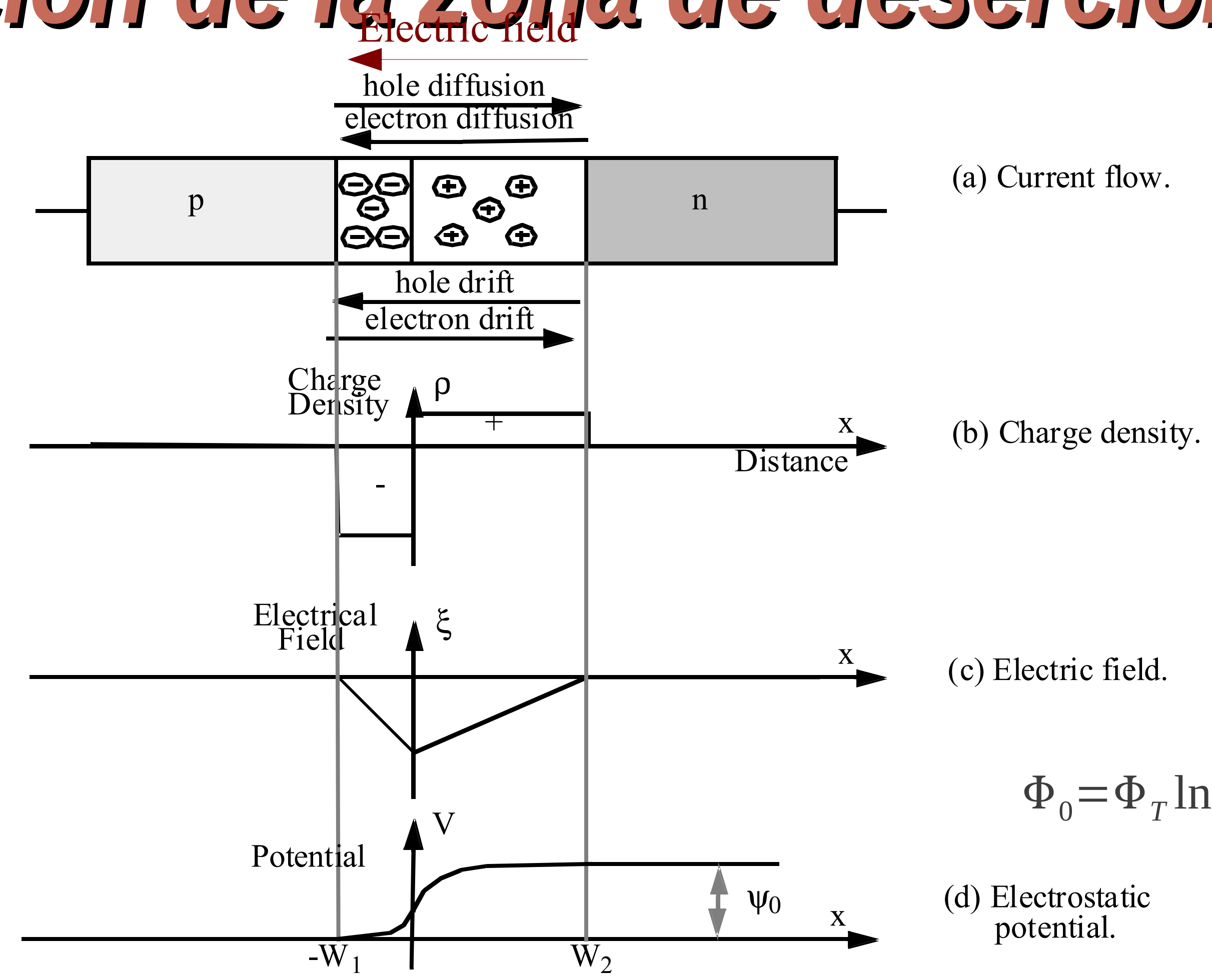
Cross-section of *pn*-junction in an IC process



diode symbol

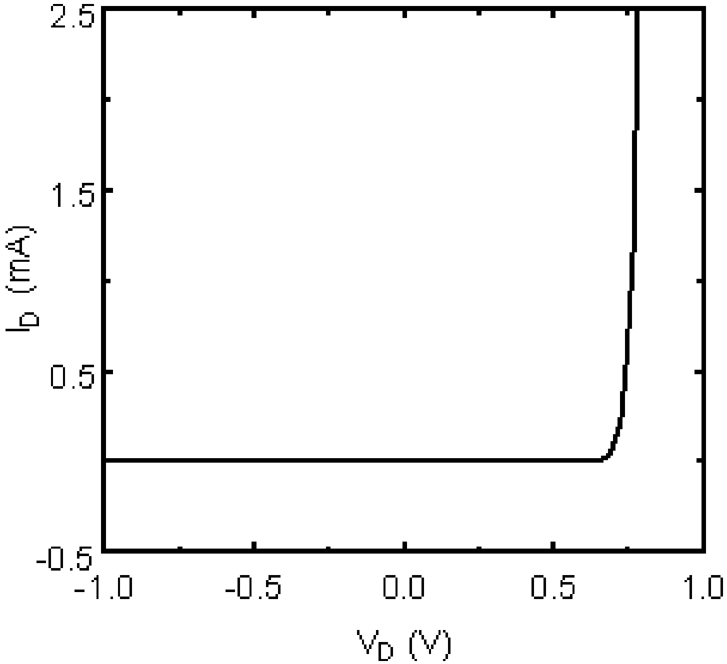
Elemento parásito en la mayor parte de los ICs digitales
Algunos usos por e.g. en protección ESD, sensores de temp., etc

Formación de la zona de deserción

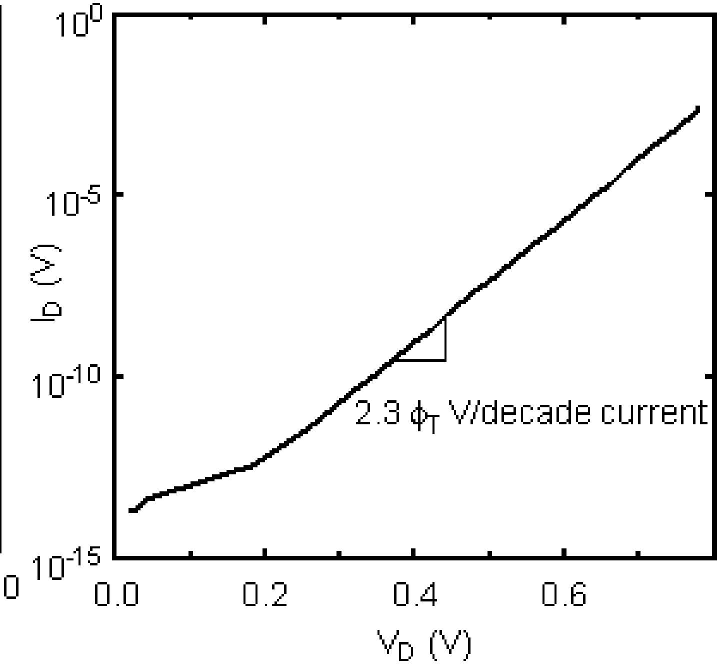


$$\Phi_0 = \Phi_T \ln\left(N_A . N_D . n_i^{-2}\right)$$

Corriente del diodo.



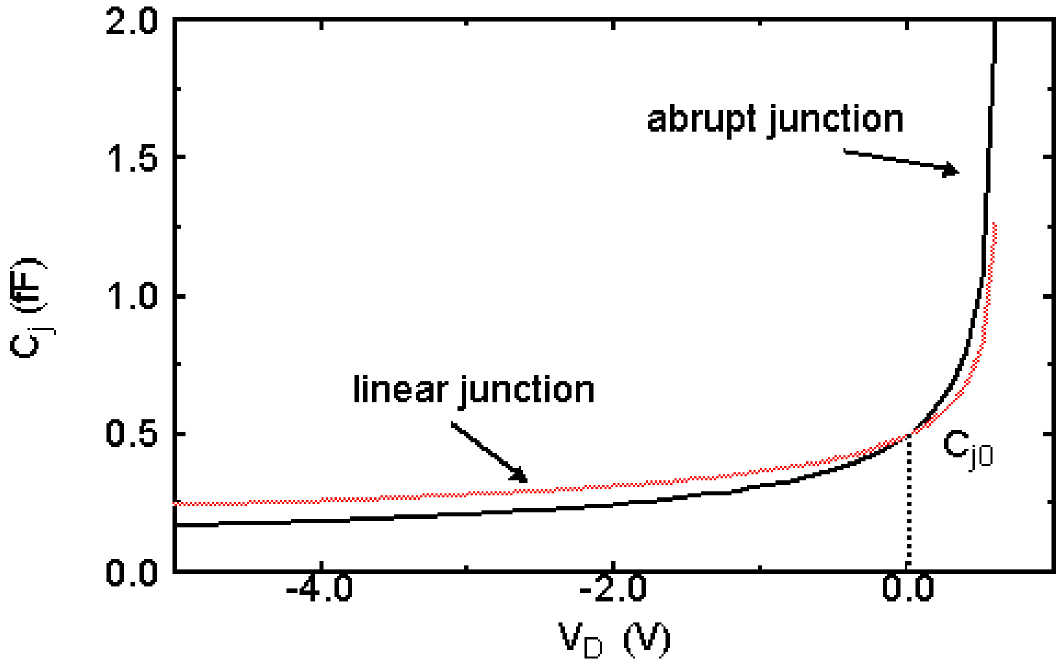
(a) On a linear scale.



(b) On a logarithmic scale (forward bias).

$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

Capacitancia de juntura



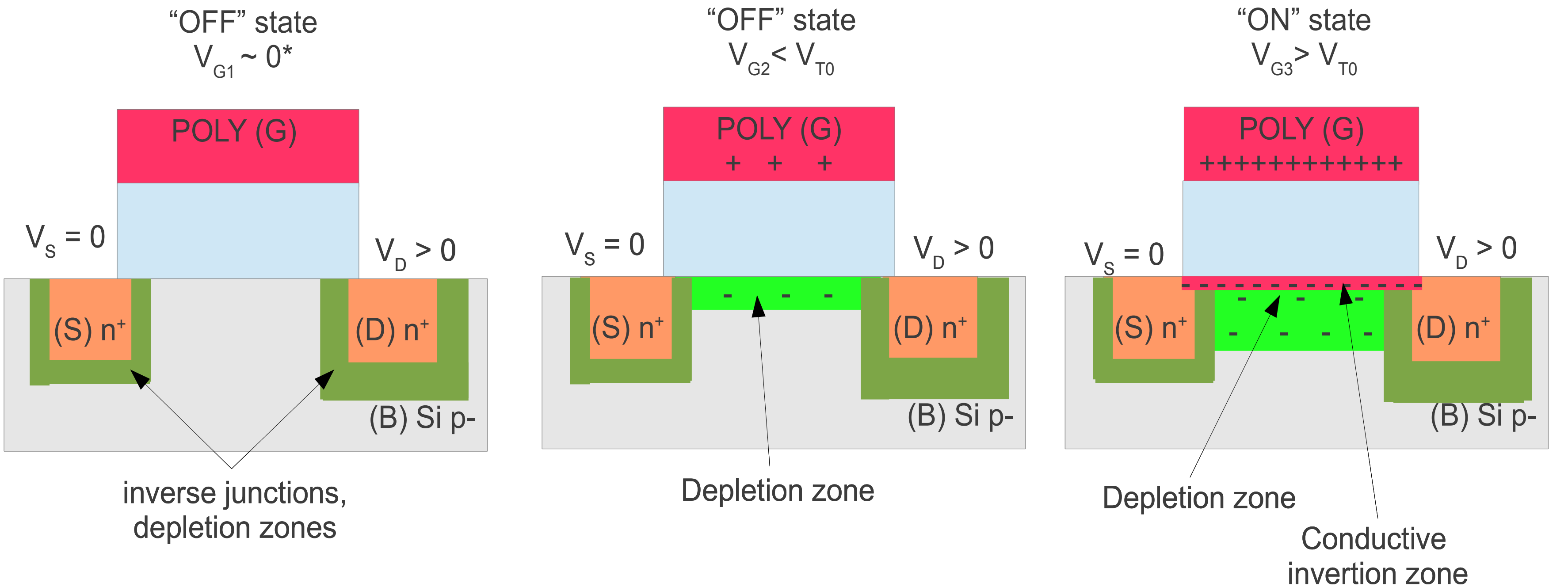
La capacitancia de inversa de junturas P-N aparece en Cdb, y esta dependencia está modelada en SPICE.

$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

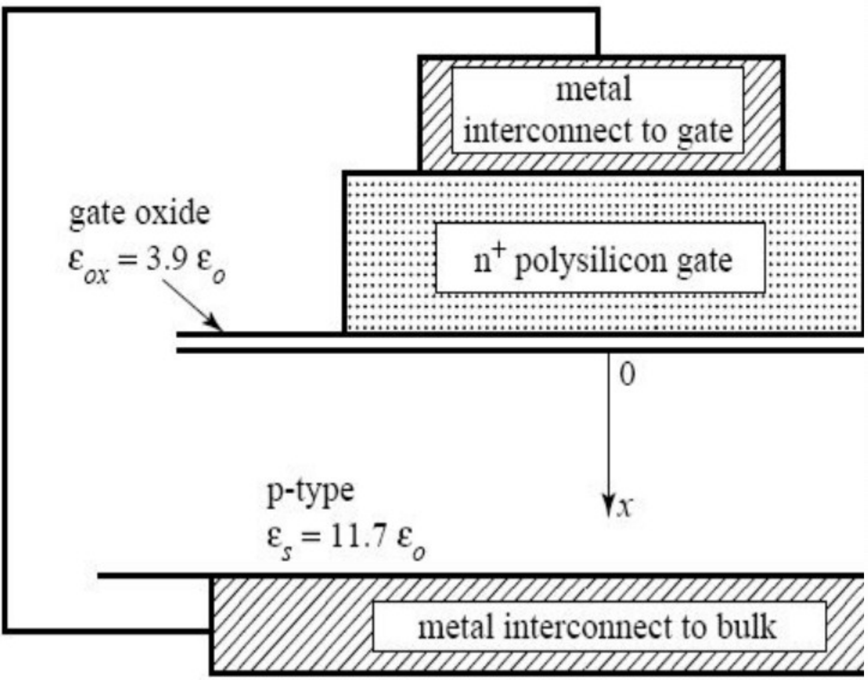
m = 0.5: abrupt junction
m = 0.33: linear junction

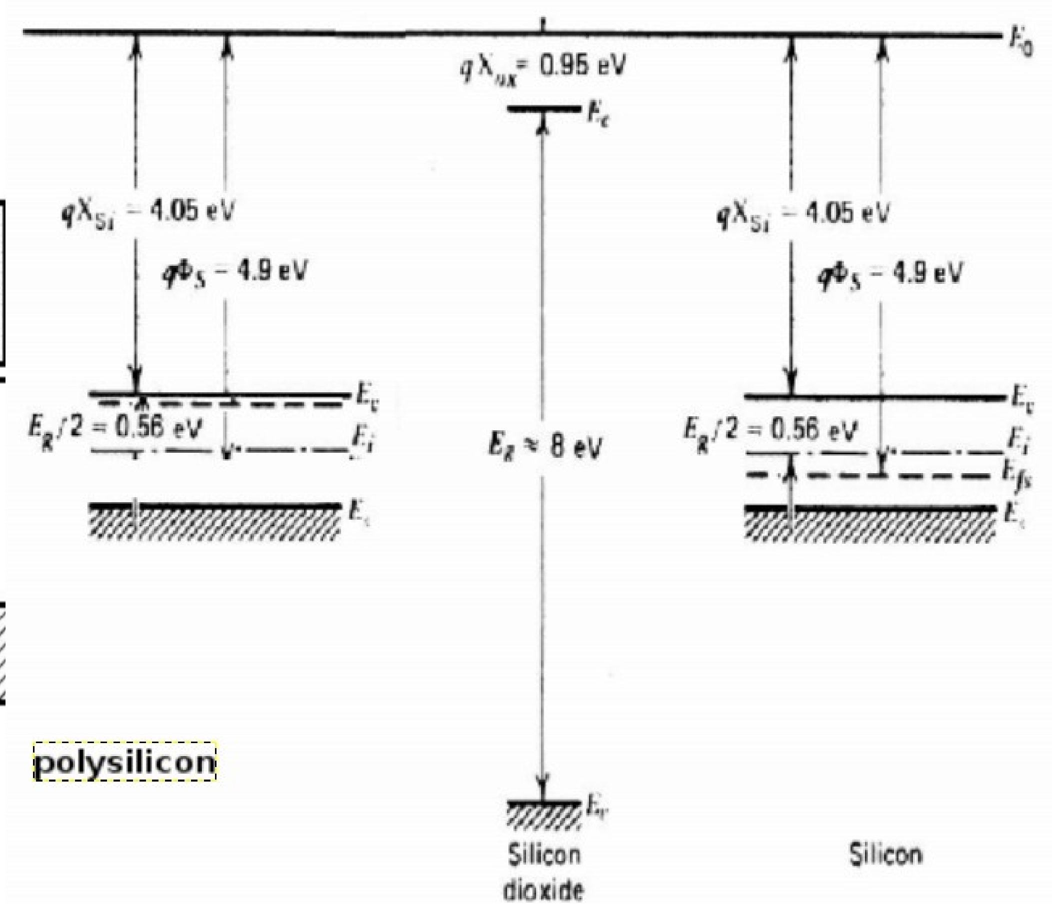
El transistor MOS, modelo naif

Fresh MOSFET:

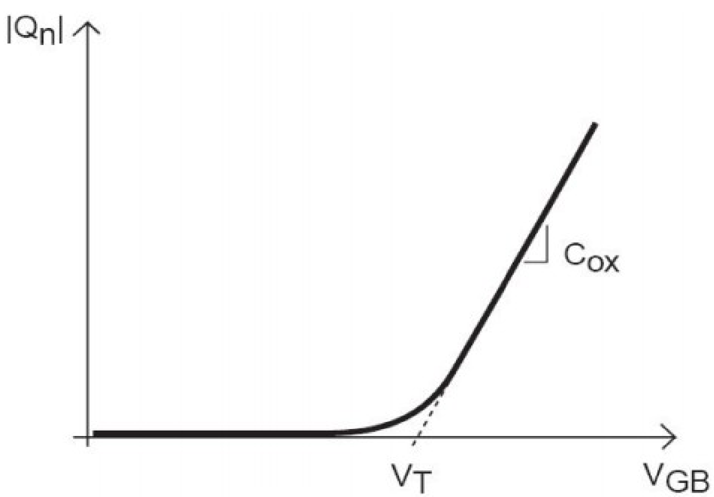


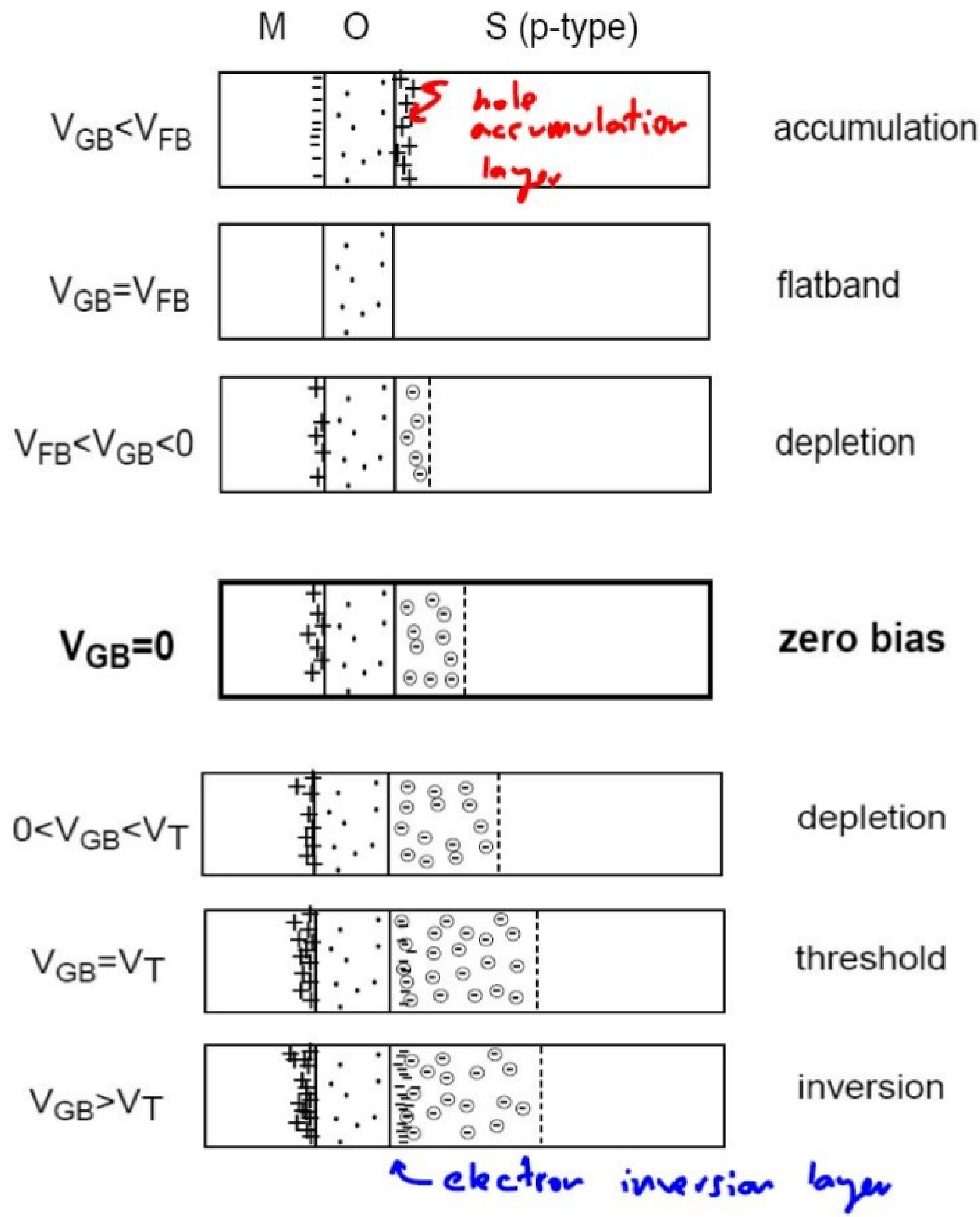
Capacitor MOS





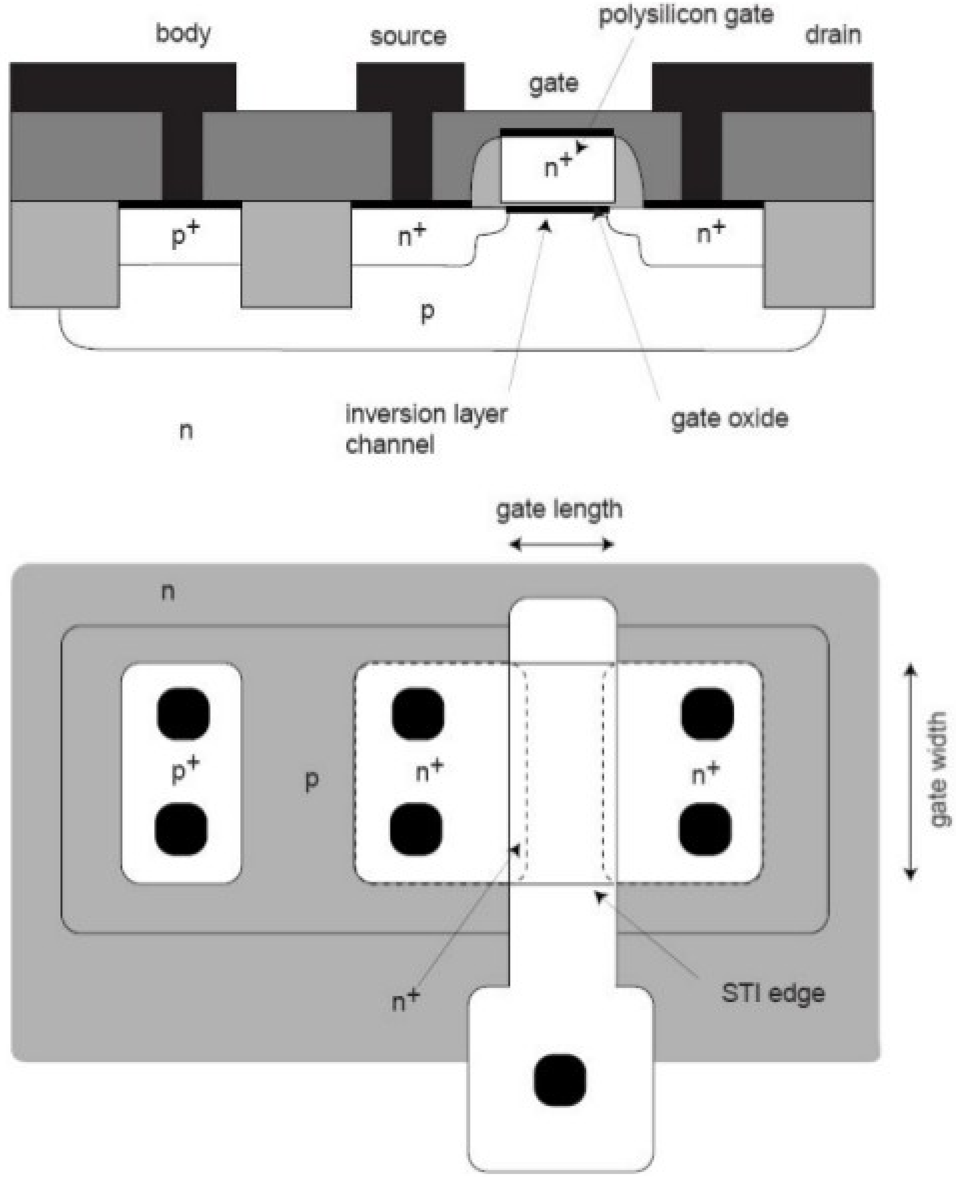
Modos de polarización



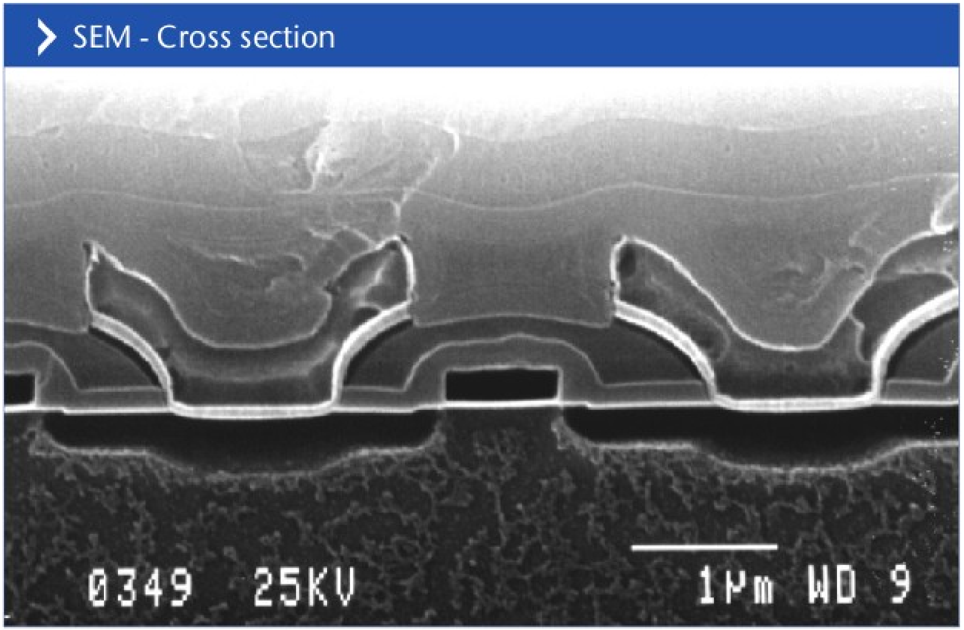


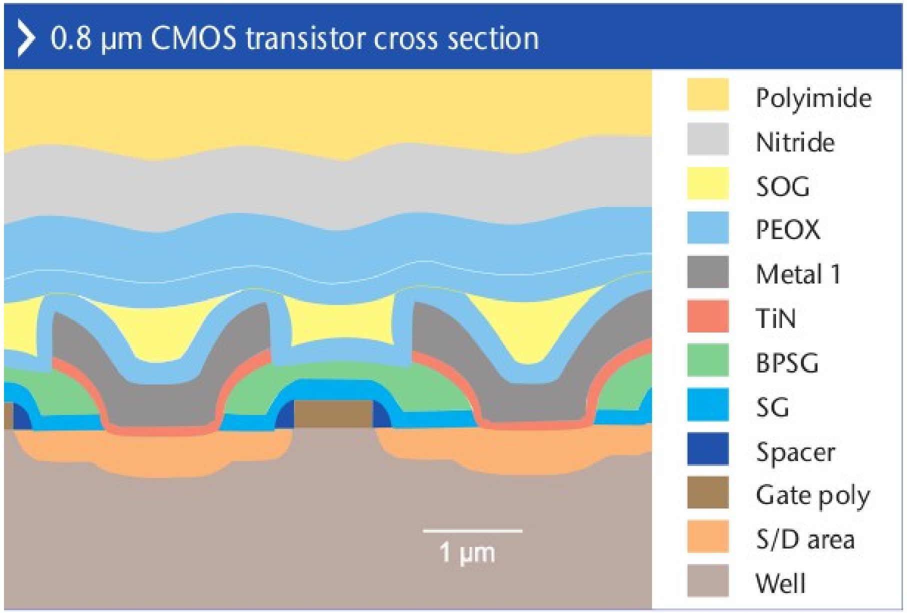
[MIT Open courses]

Transistor MOS, corte y layout



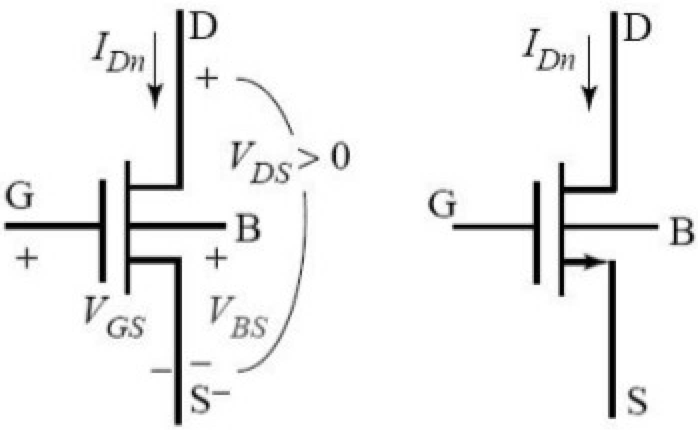
Sección real de un transistor



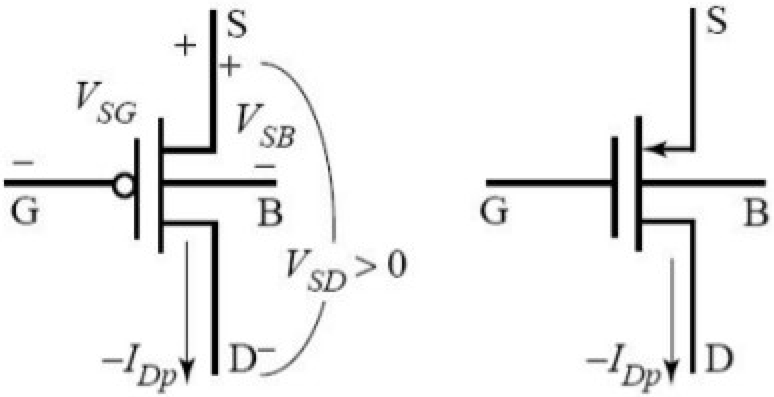


XFAB mixed signal 0.8um

Símbolos MOSFETs

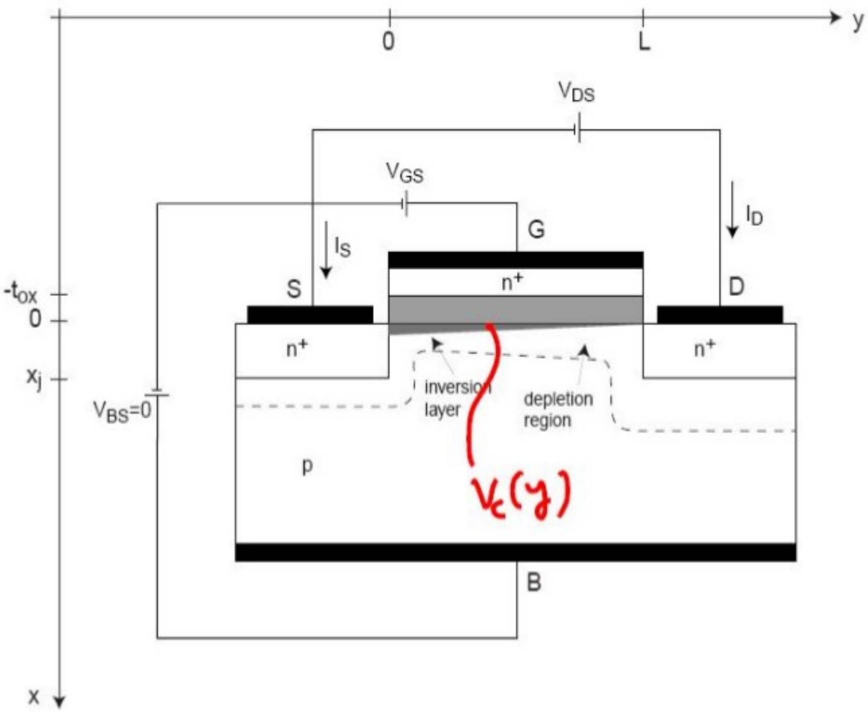


canal n



canal p

Corriente de drain.



La corriente es uniforme y fluye en la dirección y:

$$I_y = WQ_n(y)v_y(y)$$

La corriente de Drain es inversa a la corriente del canal:

$$I_D = -WQ_n(y)v_y(y)$$

- Si el campo eléctrico no es demasiado grande:

$$v_y(y) \simeq -\mu_n E_y(y) = \mu_n \frac{dV_c(y)}{dy}$$

- Para $Q_n(y)$ usamos la relación de control de carga:

$$Q_n(y) = -C_{ox}[V_{GS} - V_c(y) - V_T]$$

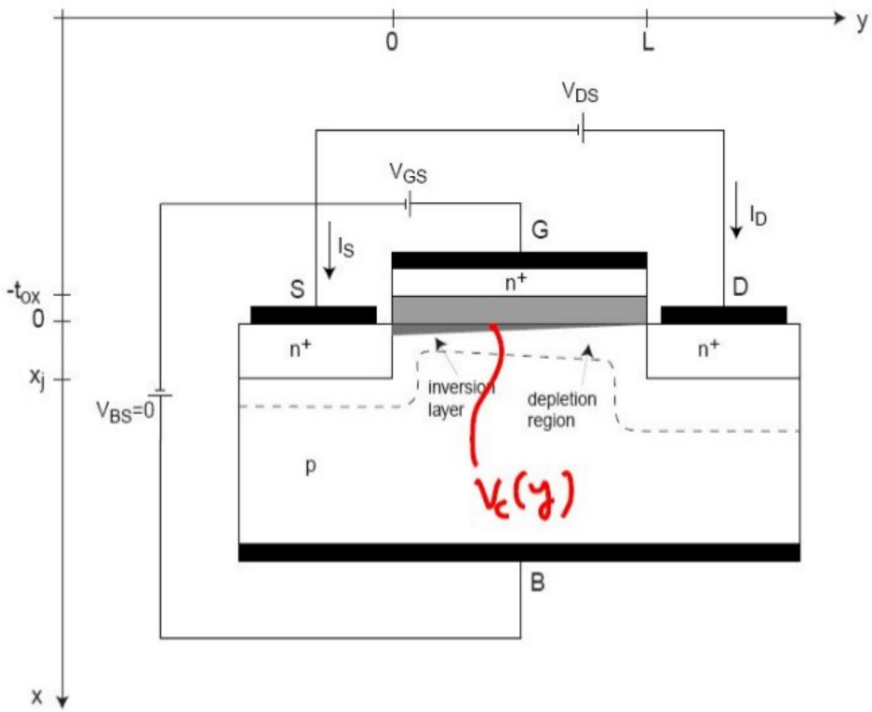
para $V_{GS} - V_c(y) \geq V_T$.

Todo junto:

$$I_D = W\mu_n C_{ox}(V_{GS} - V_c(y) - V_T)\frac{dV_c(y)}{dy}$$

Corriente de Drain

$$I_D dy = W\mu_n C_{ox}(V_{GS} - V_c - V_T)dV_c$$



Considerando regimen lineal integramos a lo largo del canal:

-para $y = 0$, $V_c(0) = 0$

-para $y = L$, $V_c(L) = V_{DS}$ (regimen lineal)

Entonces:

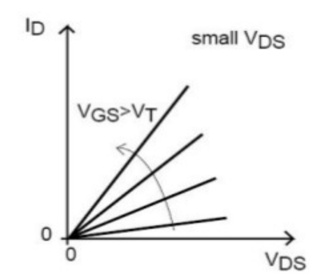
$$I_D \int_0^L dy = W\mu_n C_{ox} \int_0^{V_{DS}} (V_{GS} - V_c - V_T)dV_c$$

o:

$$I_D = \frac{W}{L}\mu_n C_{ox}(V_{GS} - \frac{V_{DS}}{2} - V_T)V_{DS}$$

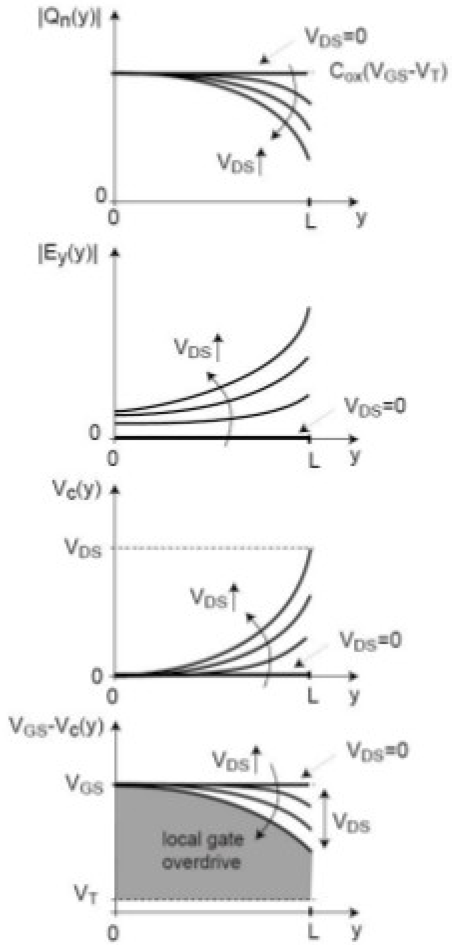
Para V_{DS} pequeña:

$$I_D \simeq \frac{W}{L}\mu_n C_{ox}(V_{GS} - V_T)V_{DS}$$

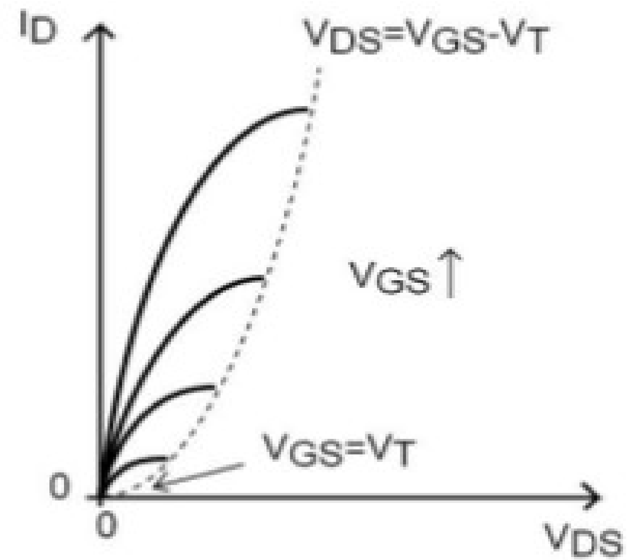


Corriente de Drain.

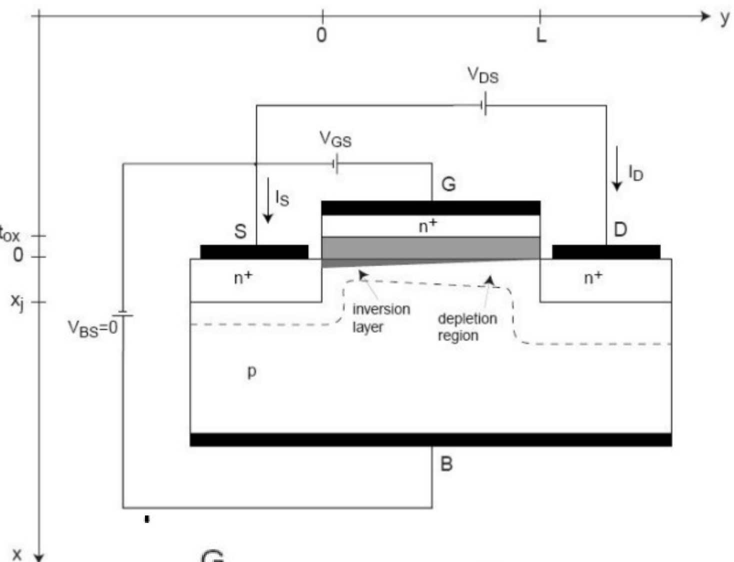
Impacto de V_{DS}:

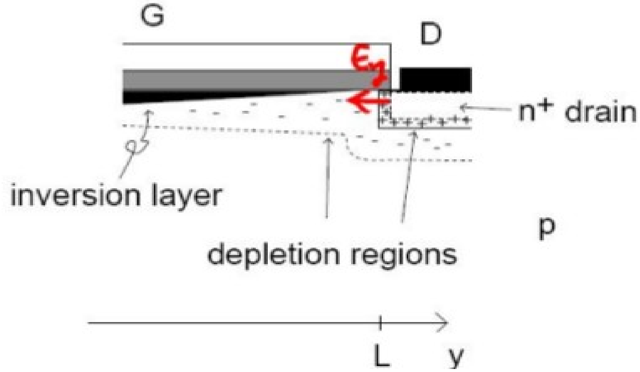


$$V_{DS} \leq V_{GS} - V_T$$



Saturación de corriente de drain





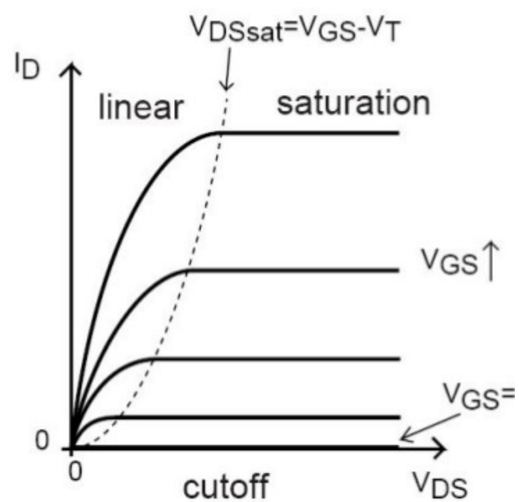
□ ¿Qué ocurre cuando $V_{DS} = V_{GS} - V_T$?
Carga del canal en el extremo del Drain:

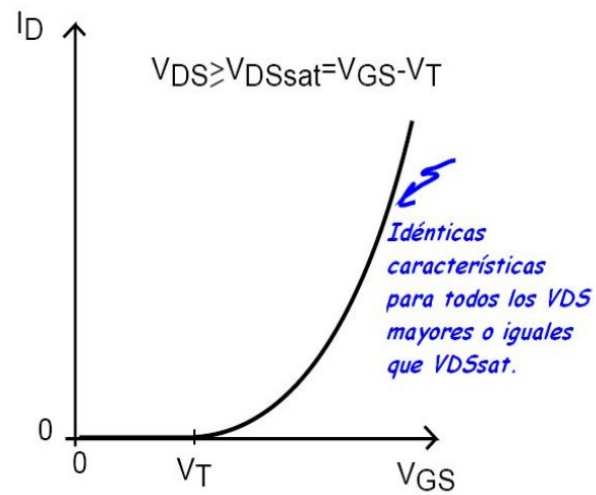
$$Q_n(L) = -C_{ox}(V_{GS} - V_{DS} - V_T) = 0$$

No hay capa de inversión en el extremo del Drain
"Pinch-off":

$$I_{Dsat} = I_{Dlin}(V_{DS} = V_{DSsat} = V_{GS} - V_T)$$

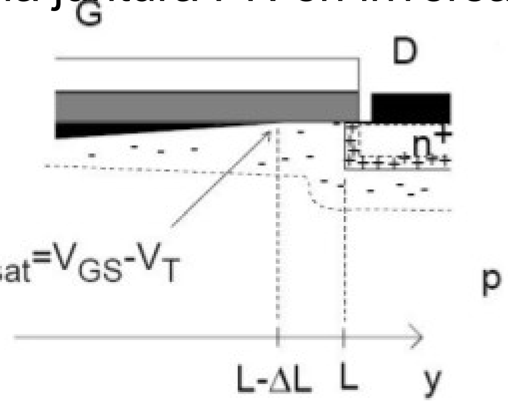
$$I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_T)^2$$





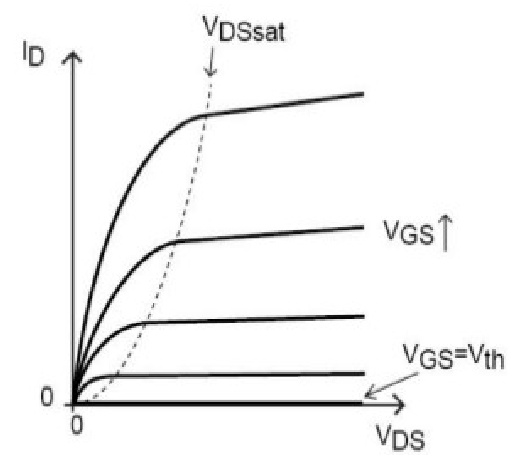
Modulación de Id con Vds

Al variar Vds la región de pinch off se alarga igual que una juntura PN en inversa:



La ecuación de ID en saturación es entonces:

$$I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_T)^2[1 + \lambda(V_{DS} - V_{DSsat})]$$



$$I_D \propto \frac{1}{L - \Delta L} \simeq \frac{1}{L}(1 + \frac{\Delta L}{L})$$

Experimentalmente se encuentra que:

$$\Delta L \propto V_{DS} - V_{DSsat}$$

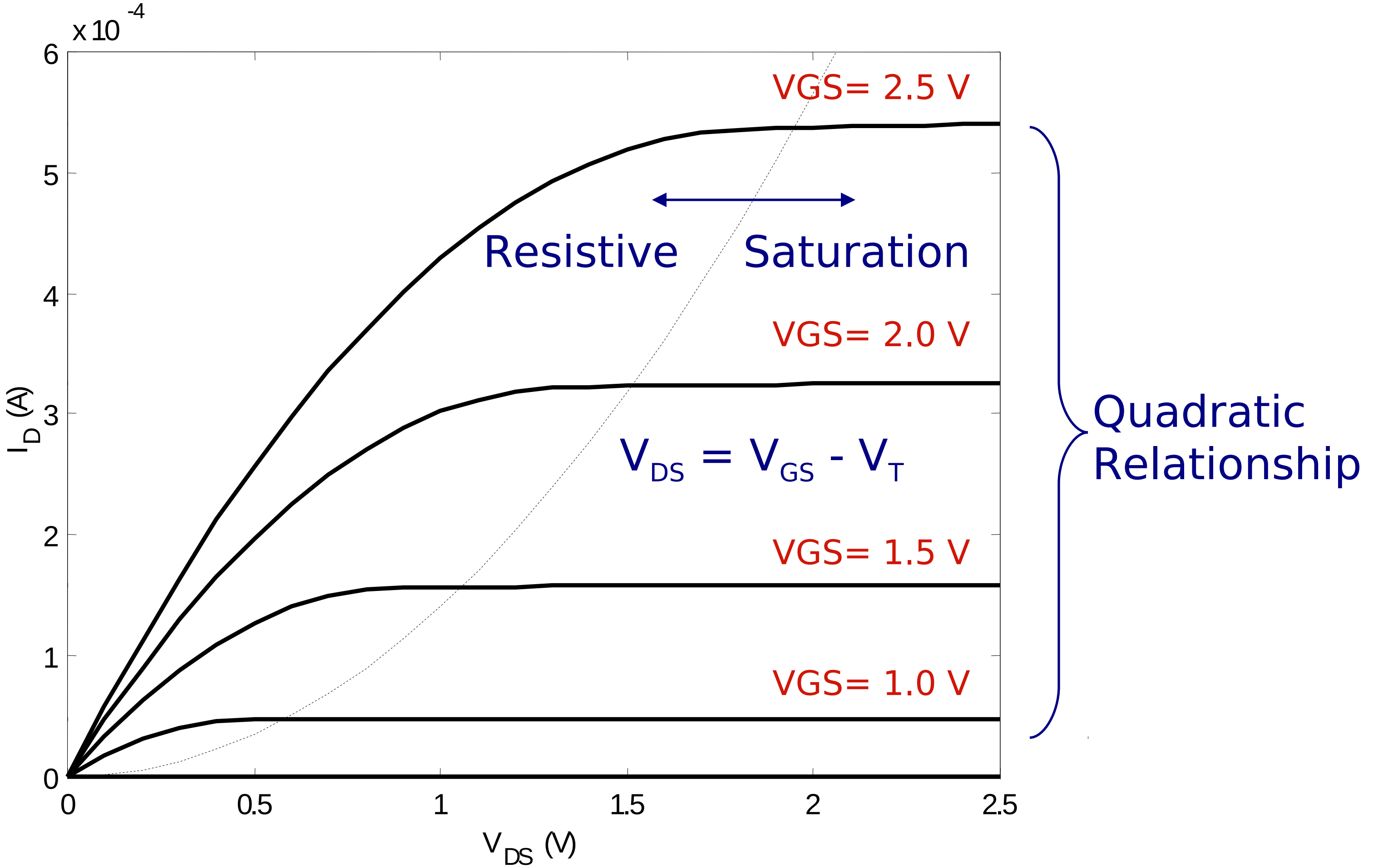
Luego:

$$\frac{\Delta L}{L} = \lambda(V_{DS} - V_{DSsat})$$

Del mismo modo, experimentalmente se encuentra que:

$$\lambda \propto \frac{1}{L}$$

I-Vs en un viejo transistor de canal largo...



Relaciones I-V para canal largo

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

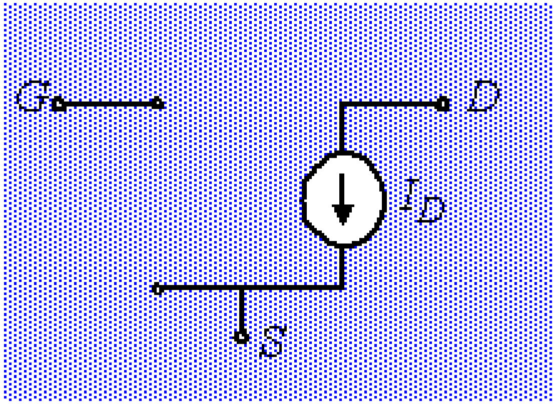
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Modelo para análisis manual



$V_{DS} > V_{GS} - V_T$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

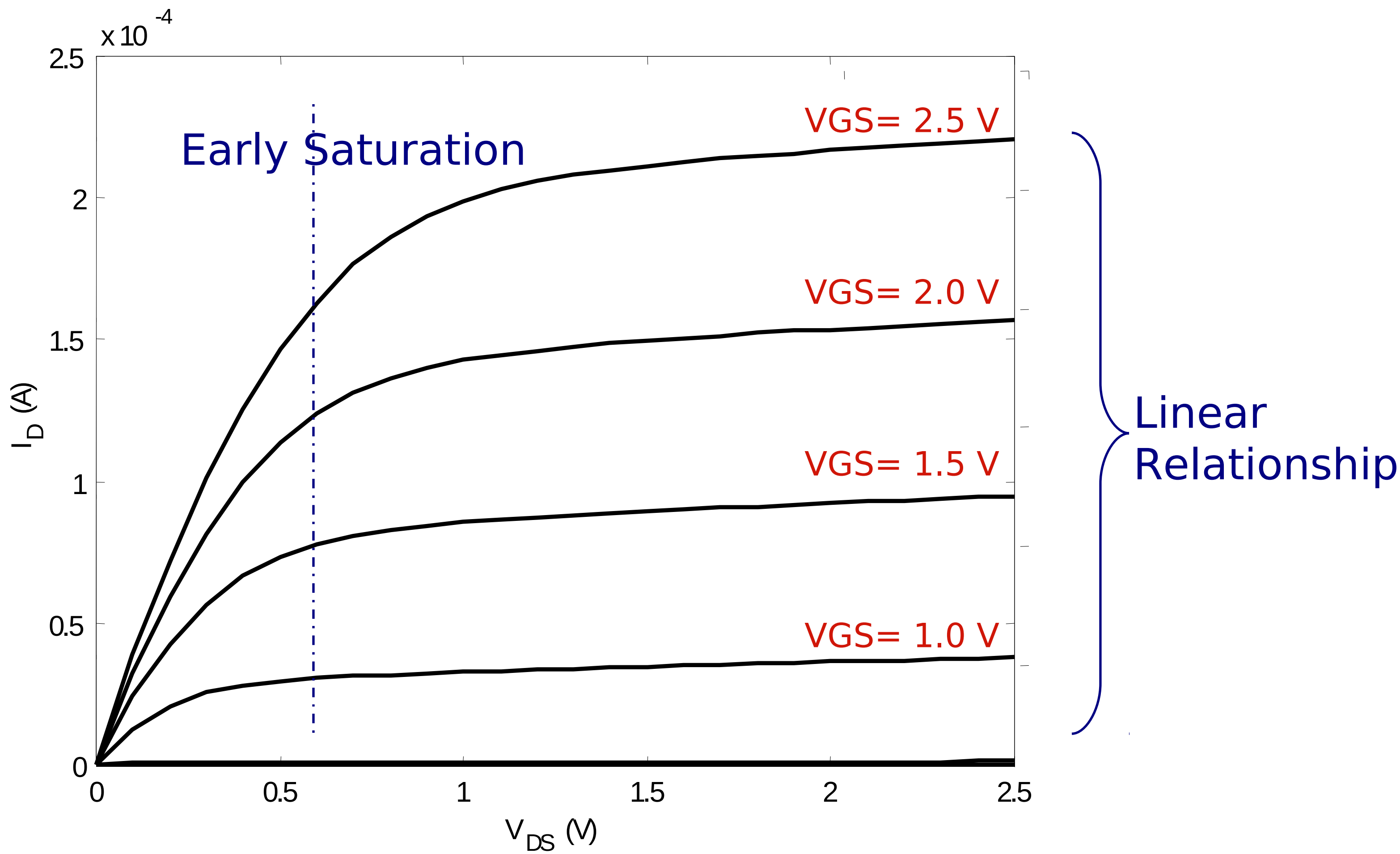
$V_{DS} < V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

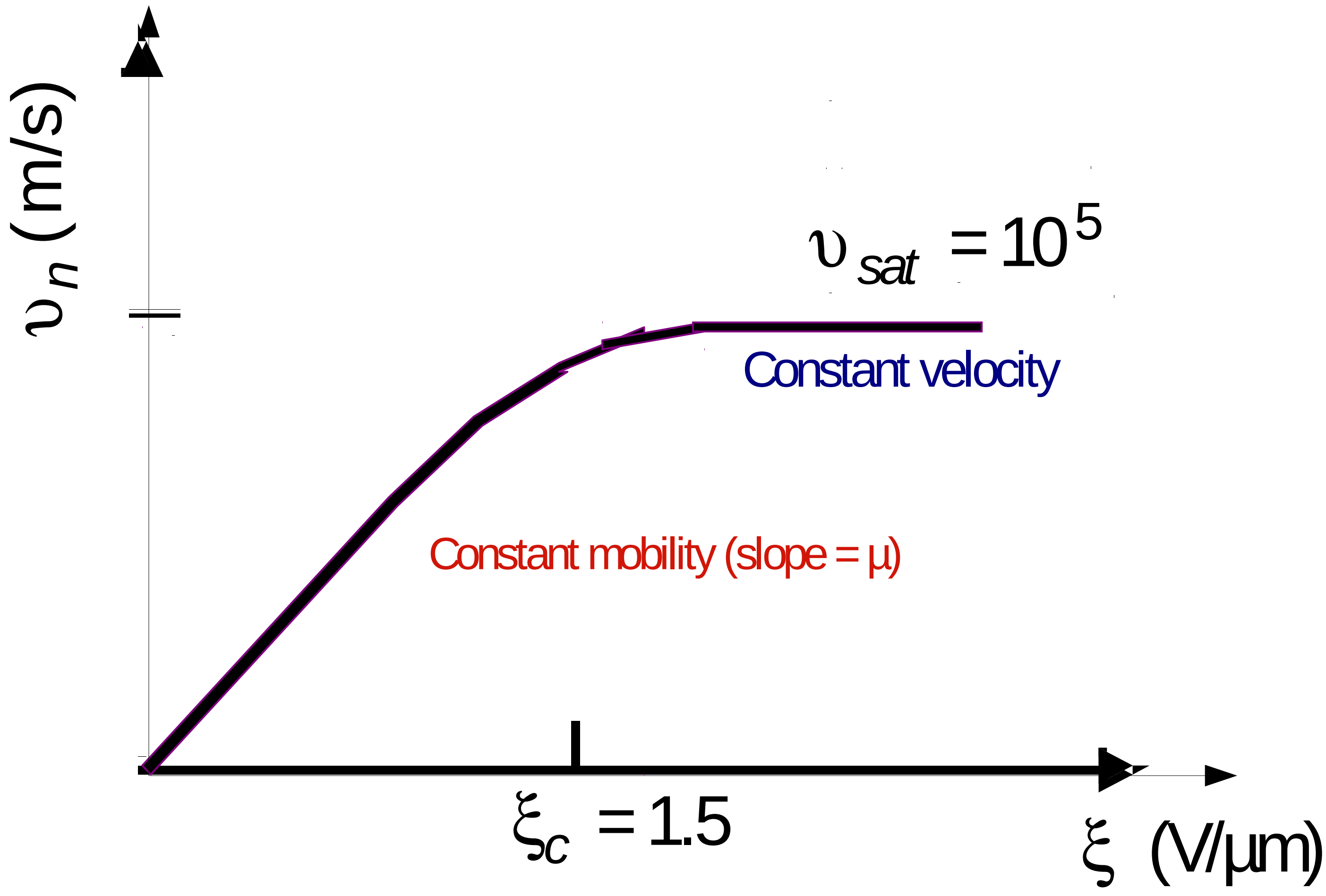
with

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

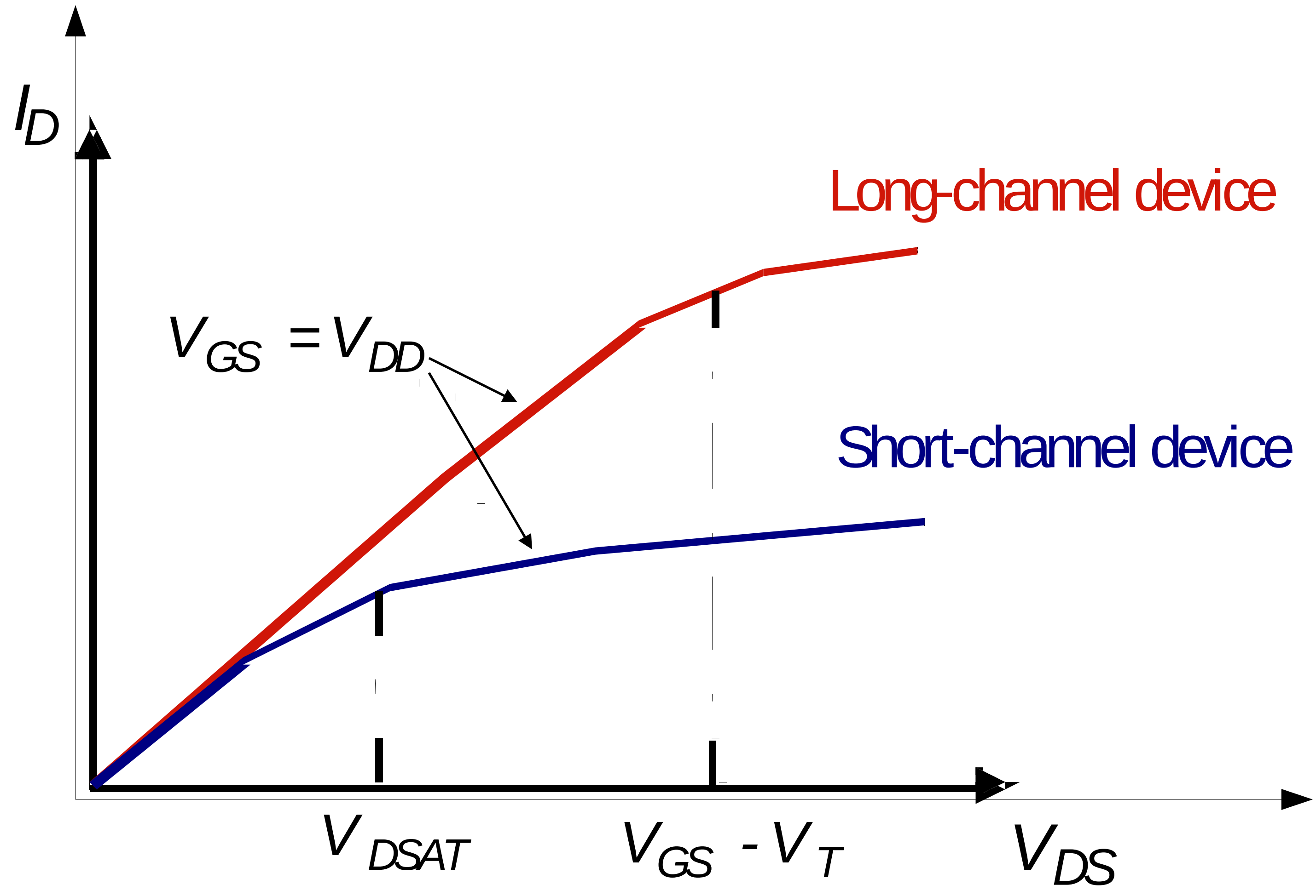
I-Vs para transistores de canal largo pero no tanto.



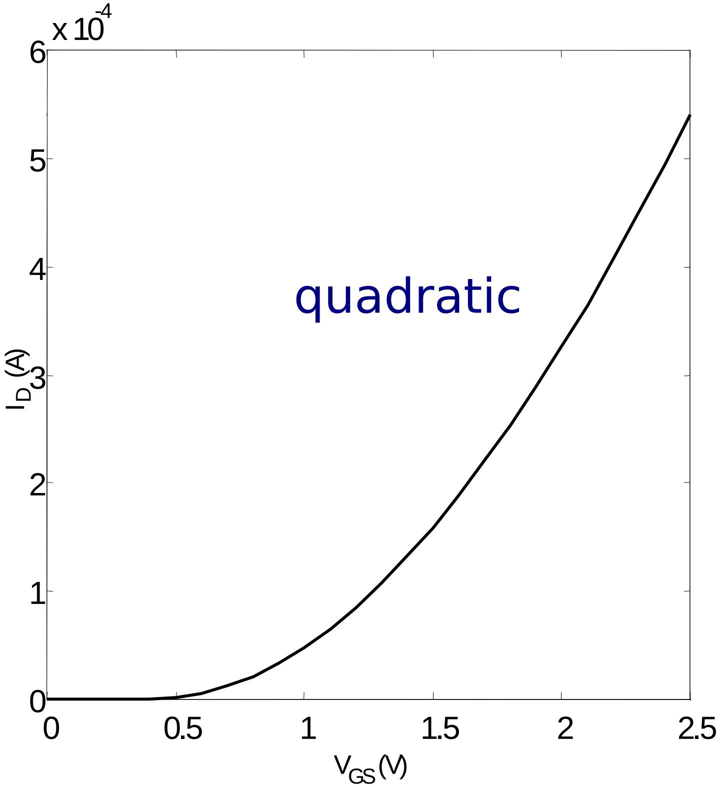
Saturación de velocidad de portadores



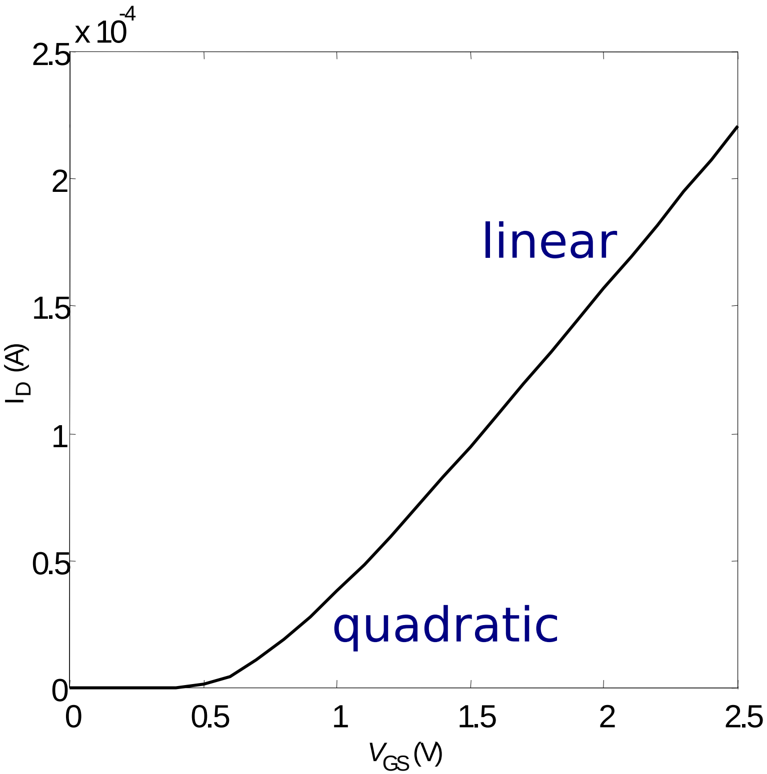
Perspectiva



I_D versus V_{GS}

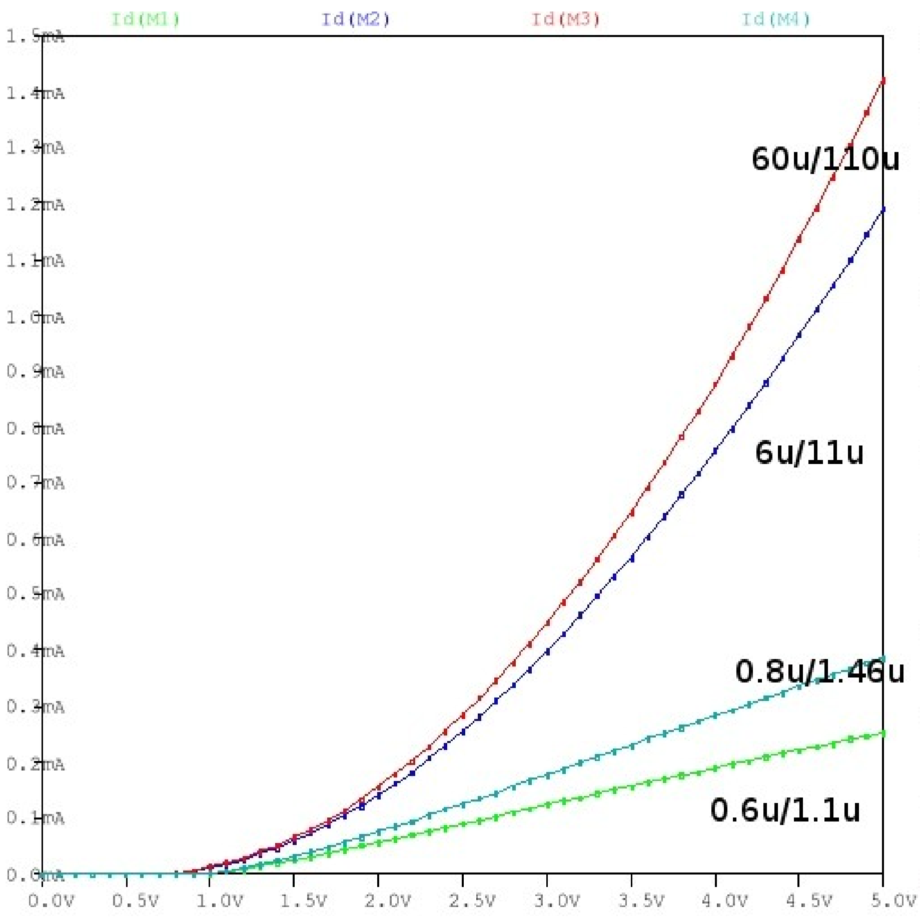


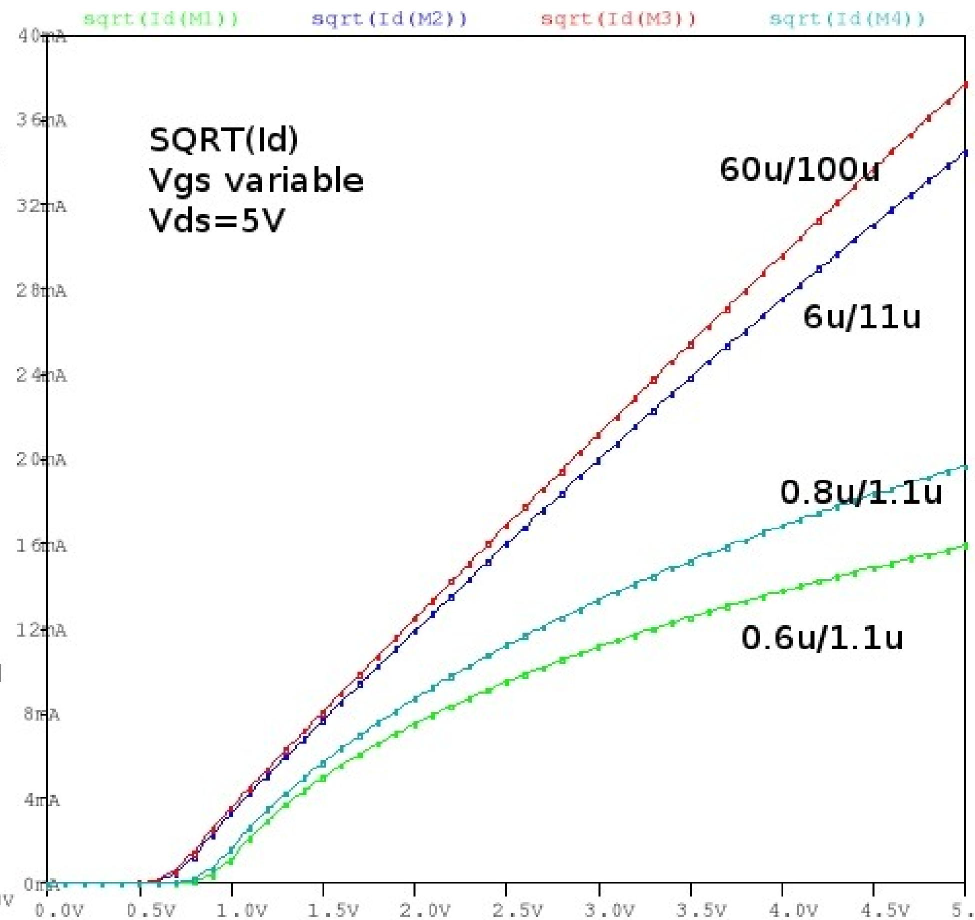
Long Channel



Short Channel

Curvas Id vs Vgs proceso 0,5um

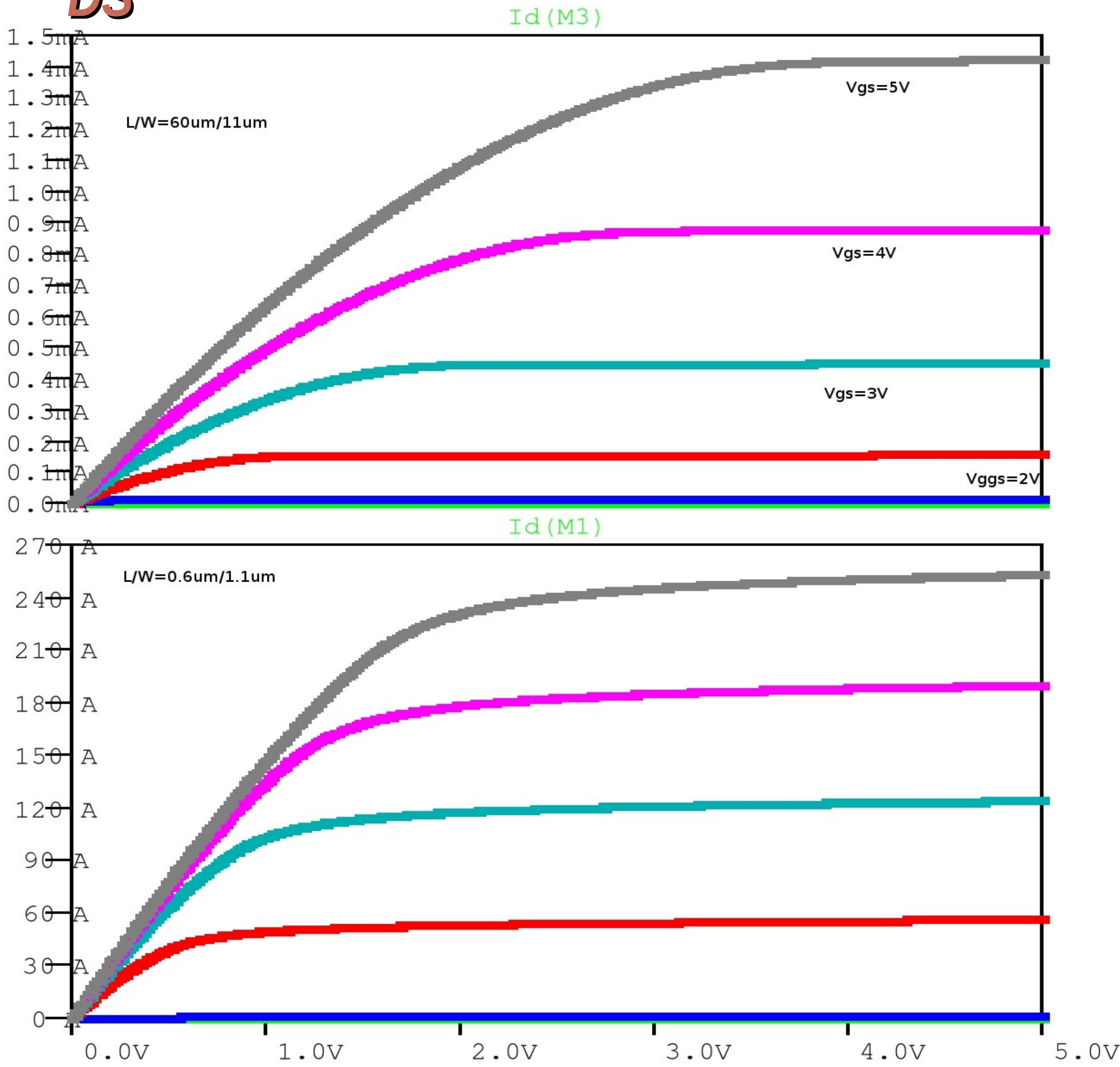




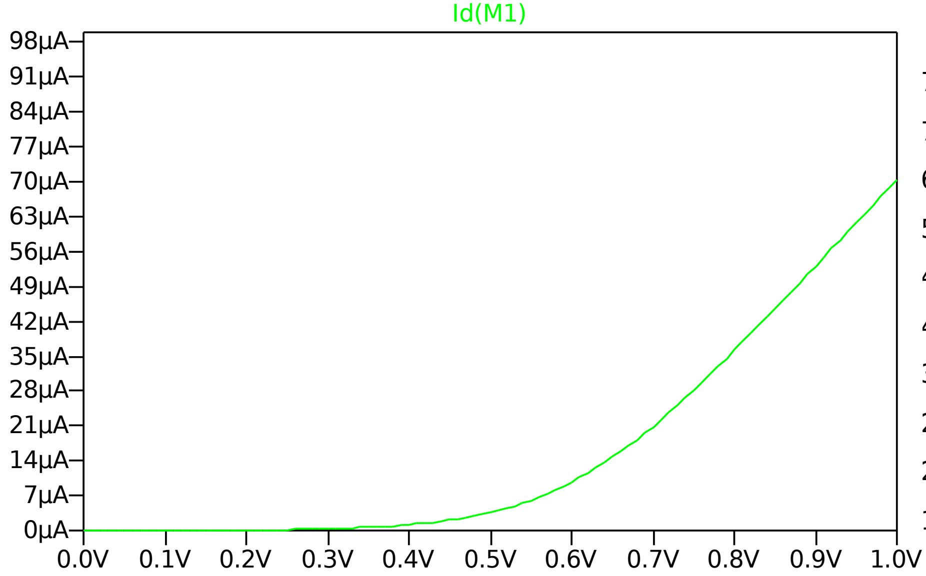
C5: I_D versus V_{DS}

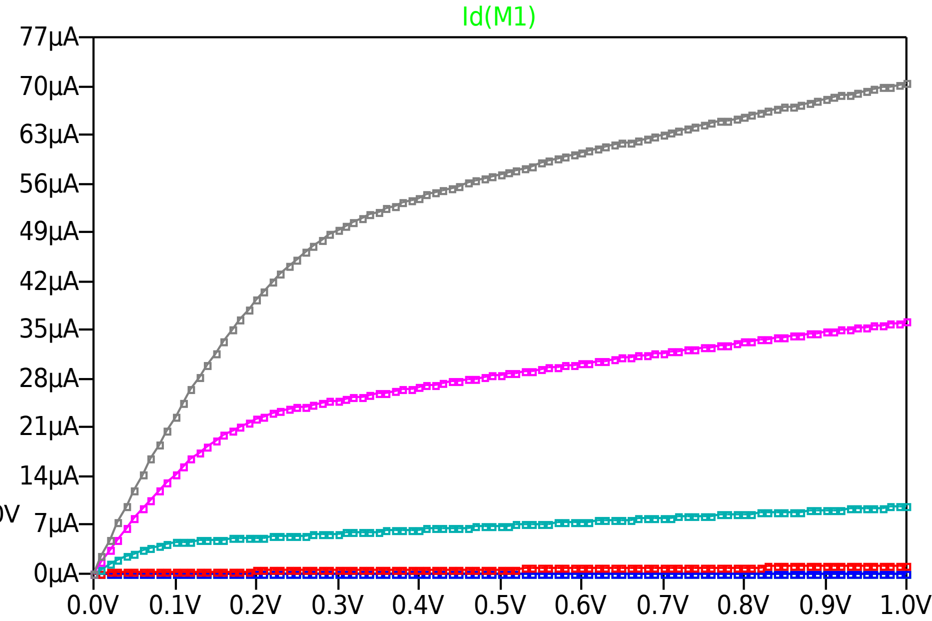
Long Channel

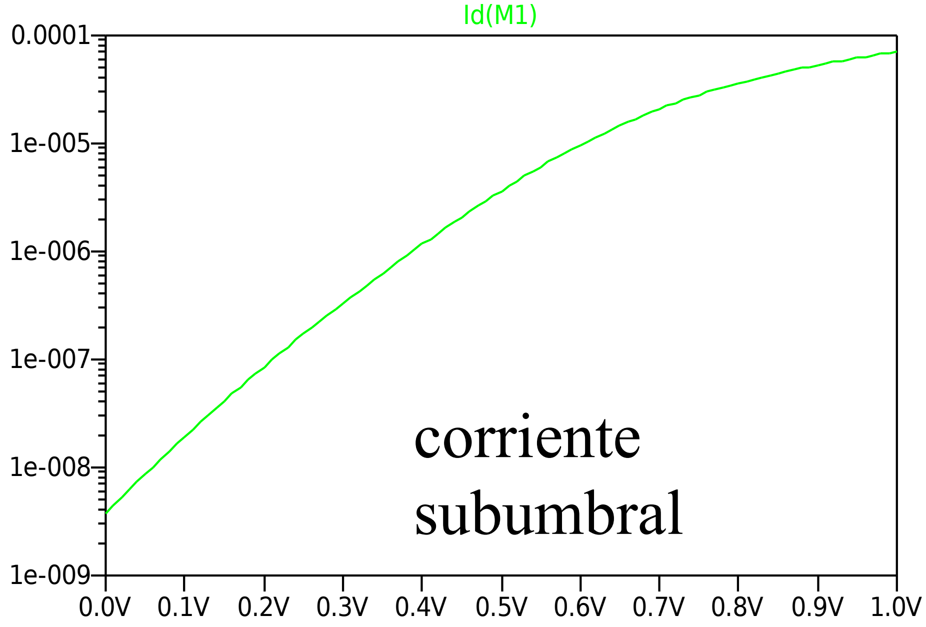
Short Channel



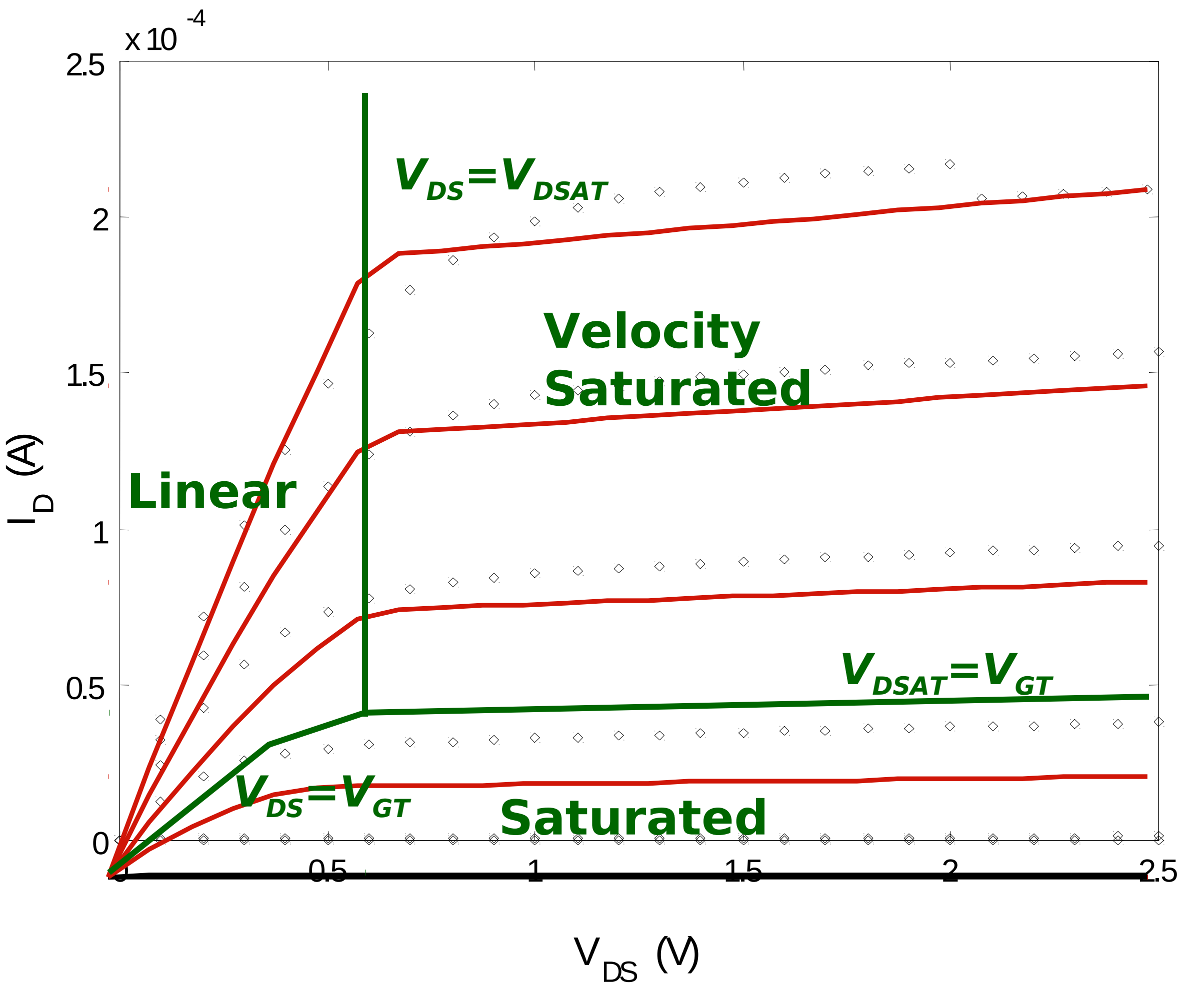
IBM 90nm, curvas IV



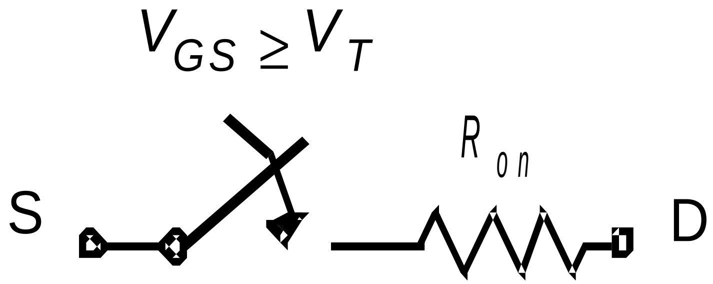


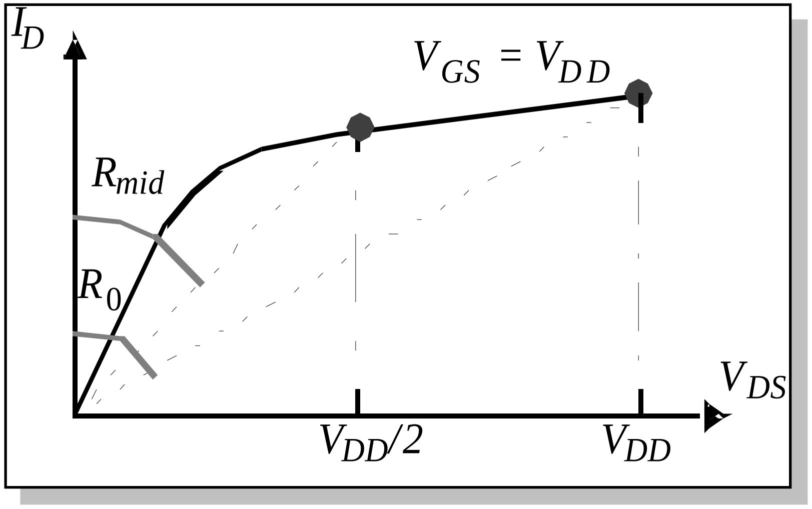


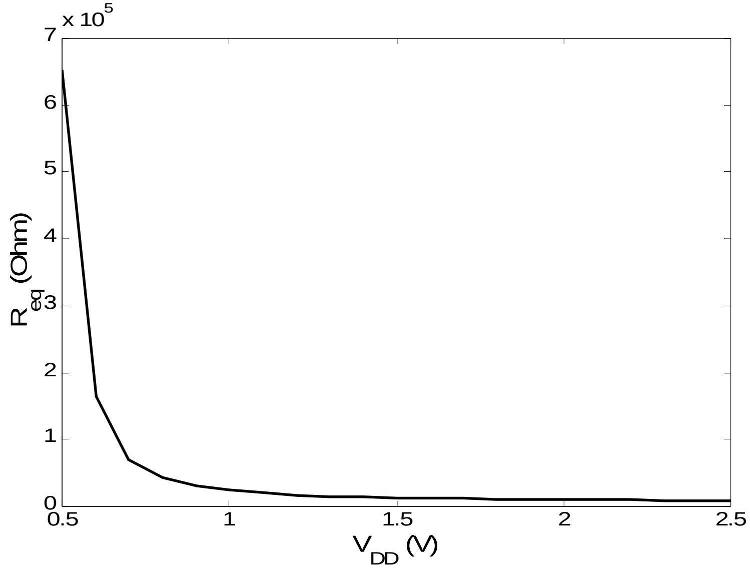
Modelo simple vs SPICE



El transistor como switch

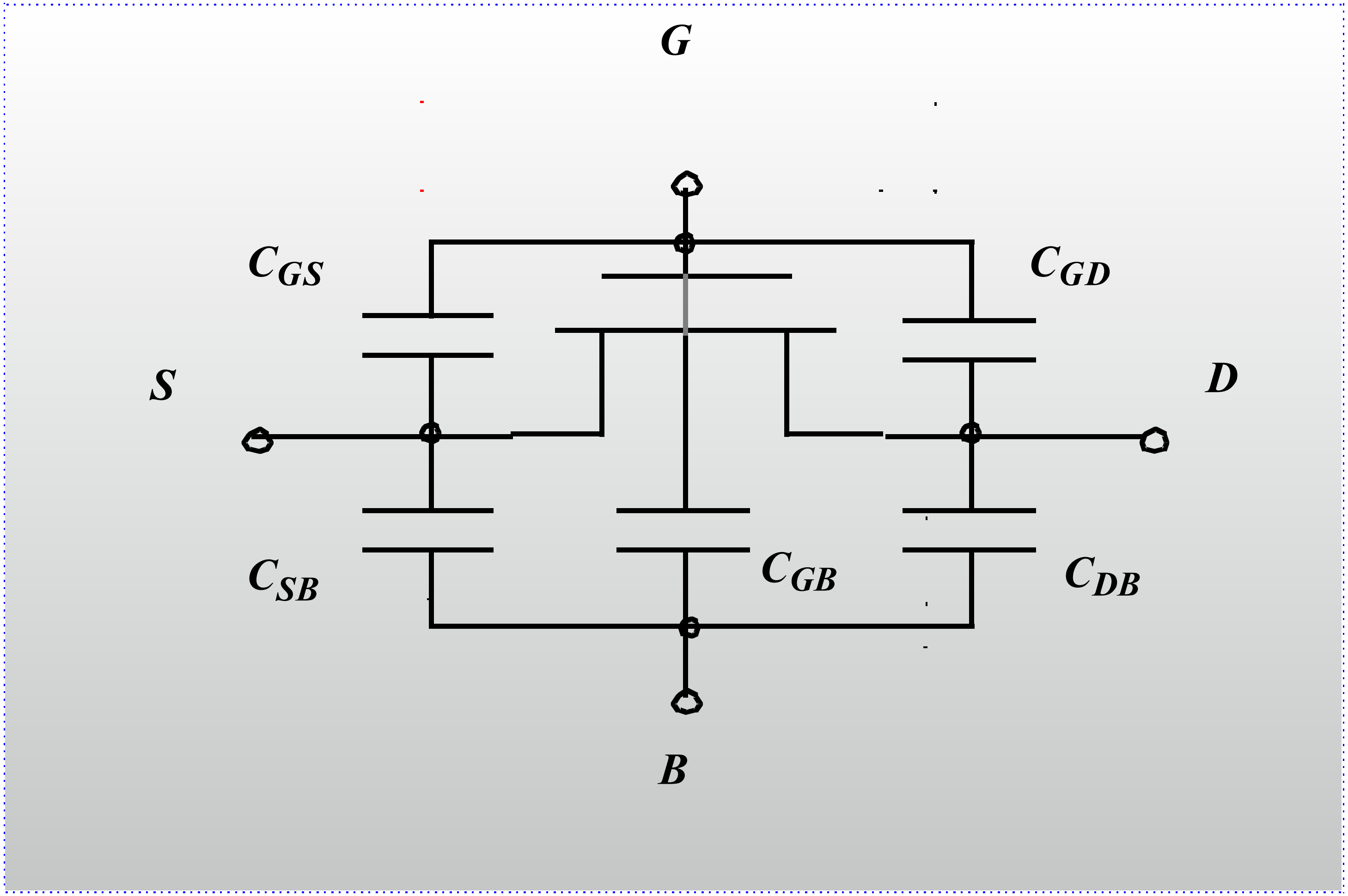




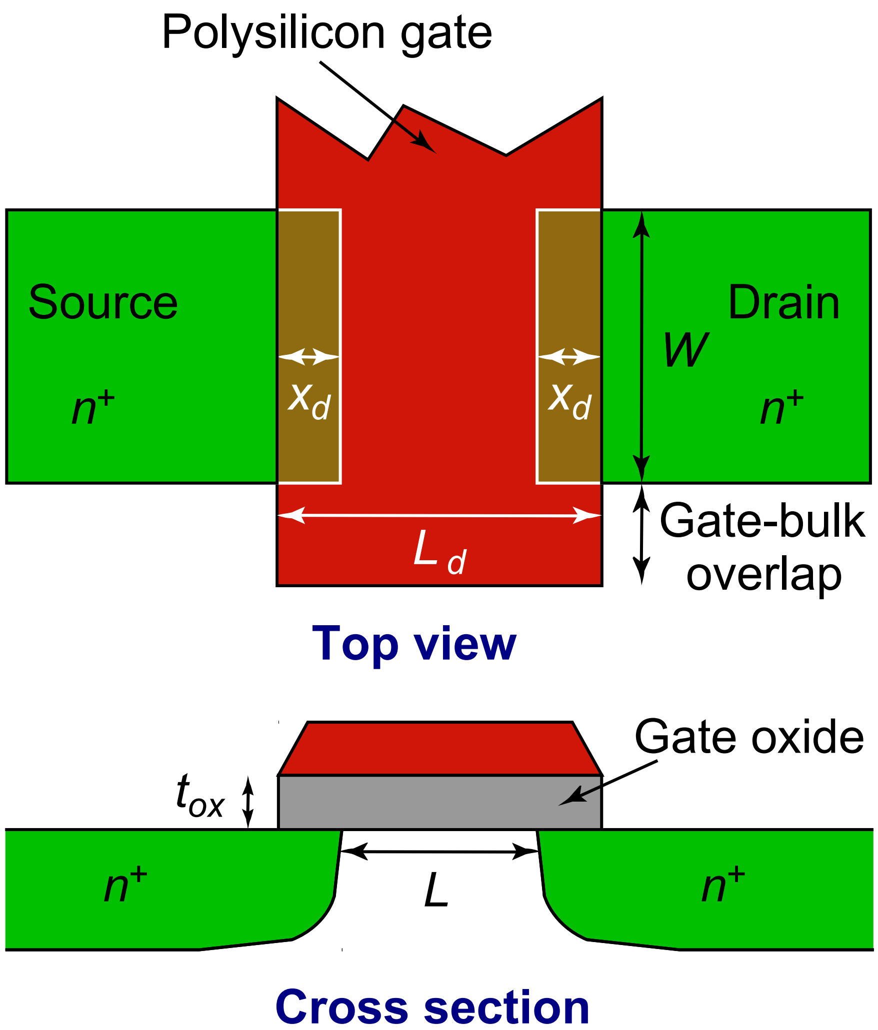


Capacitancias de pequeña señal en transistores MOS.

Dynamic Behavior of MOS Transistor

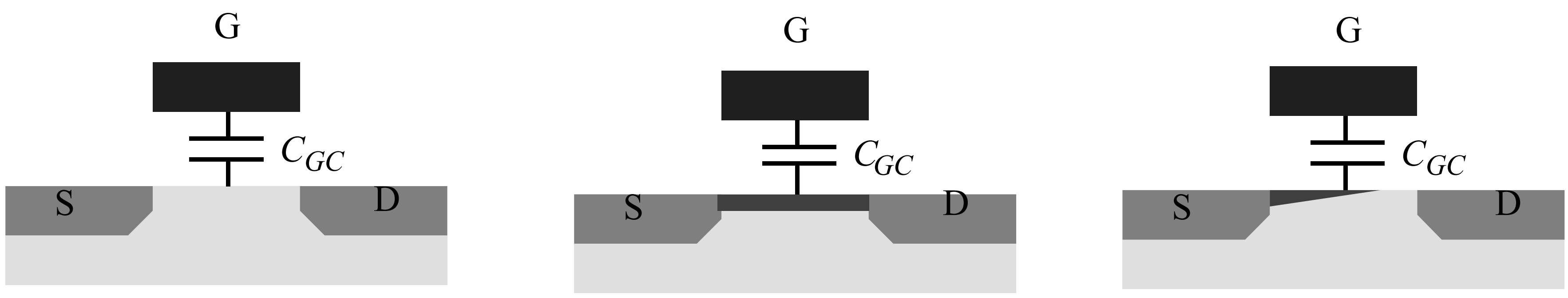


Capacitancia del gate.



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

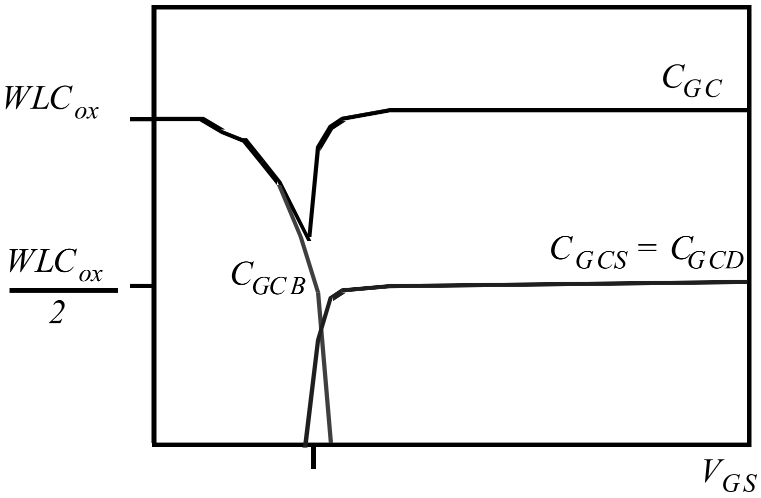
Capacitancia del gate.

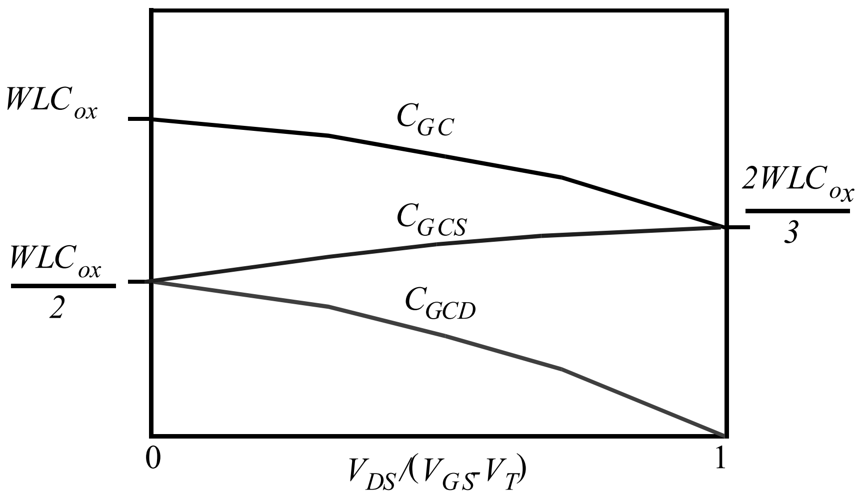


Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

Capacitancia de gate, mejor modelo.

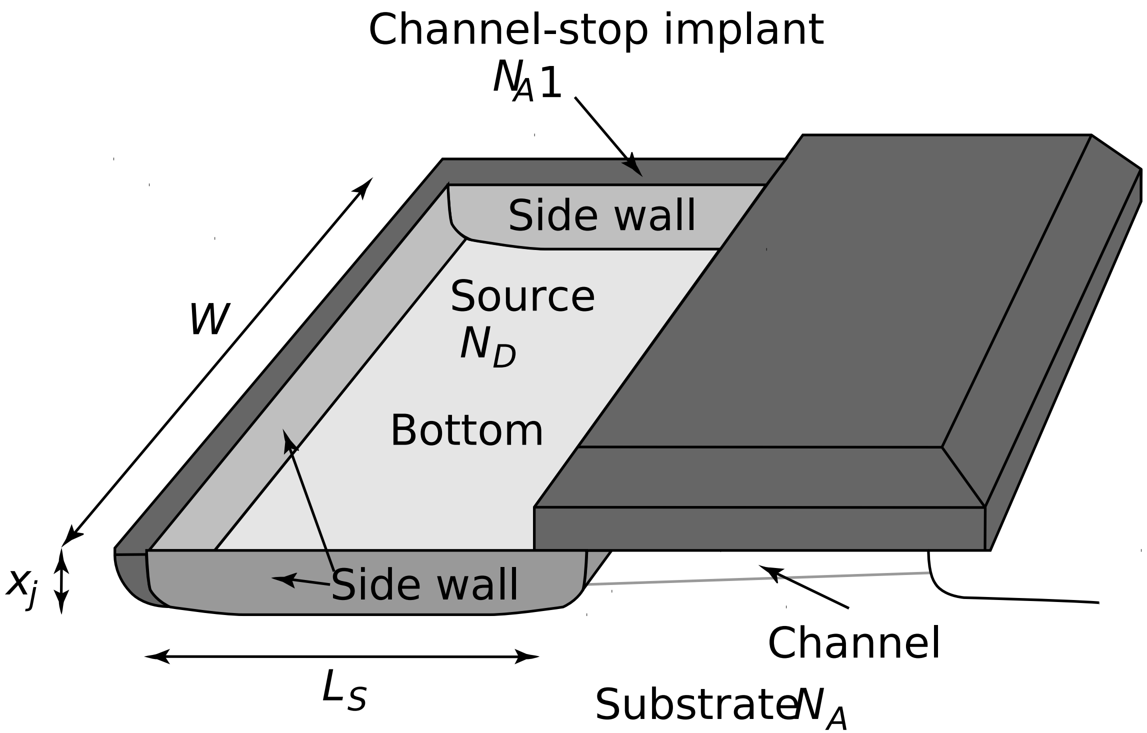




Capacitance as a function of VGS (with VDS = 0)

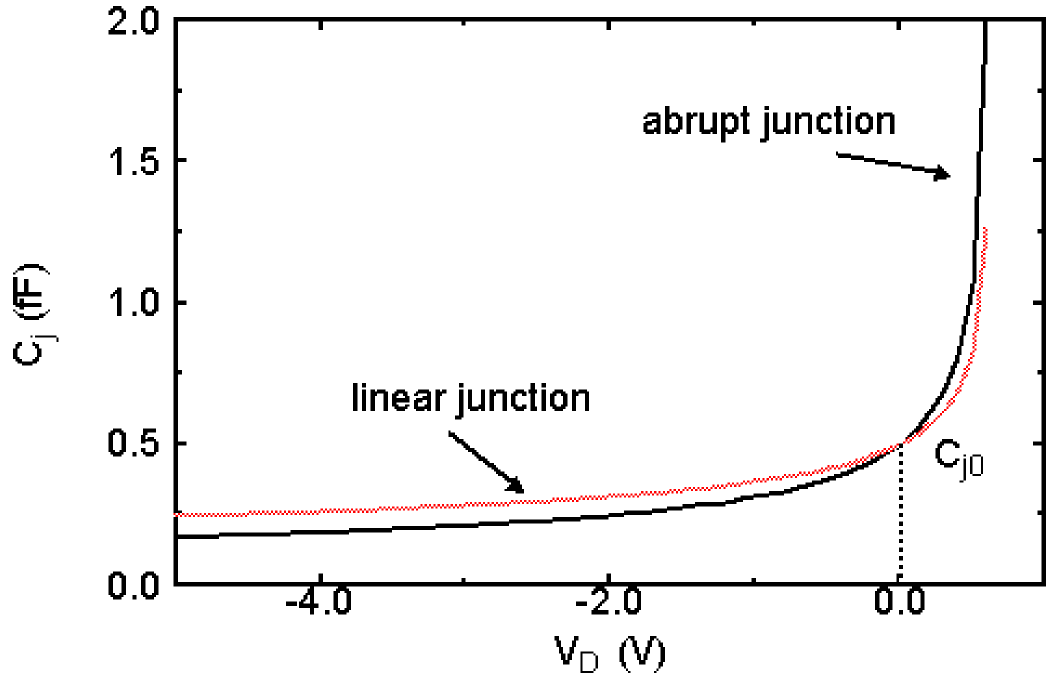
Capacitance as a function of the degree of saturation

Capacitancia de difusión.



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge
over voltage swing of interest

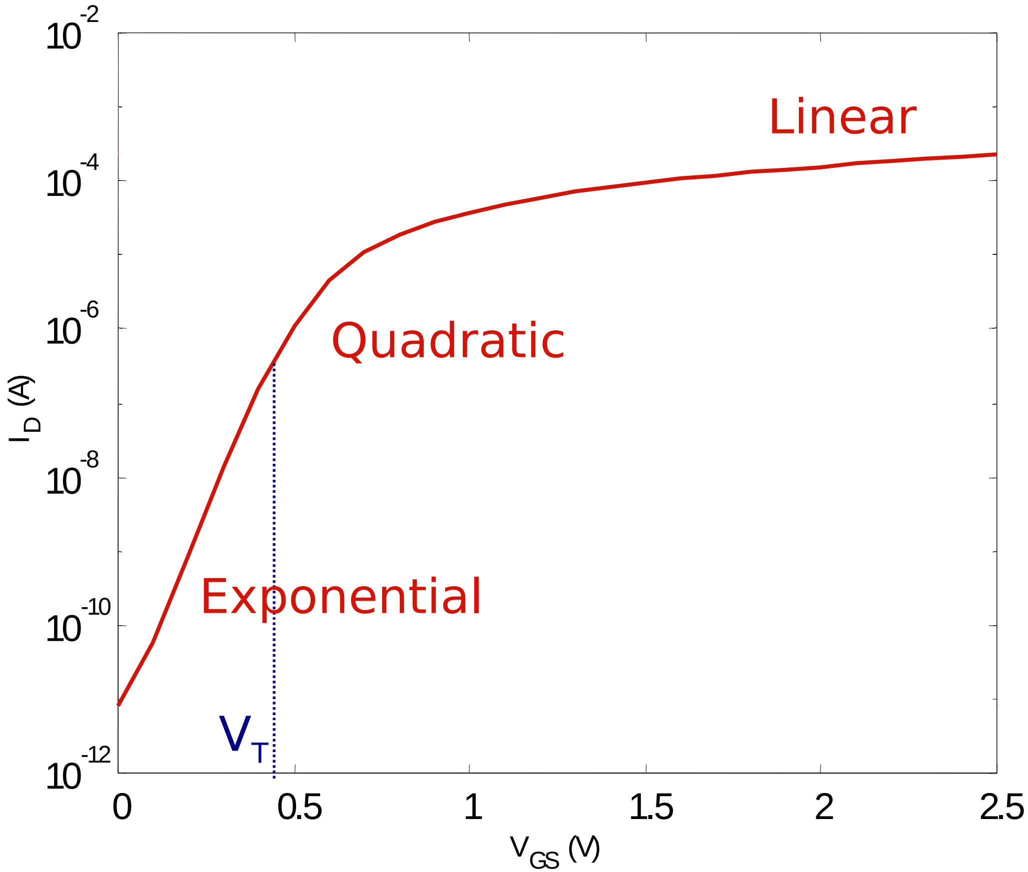
$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)}[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Capacitancias en 0.5 μm ON semi

	Cox fF/um²	Cov fF/um	Cj fF/um	mj	Cjsw fF/um
NMOS	2.4	0.18	0.41	0.43	0.14
PMOS	2.3	0.24	0.72	0.49	0.21

Conducción subumbral.



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

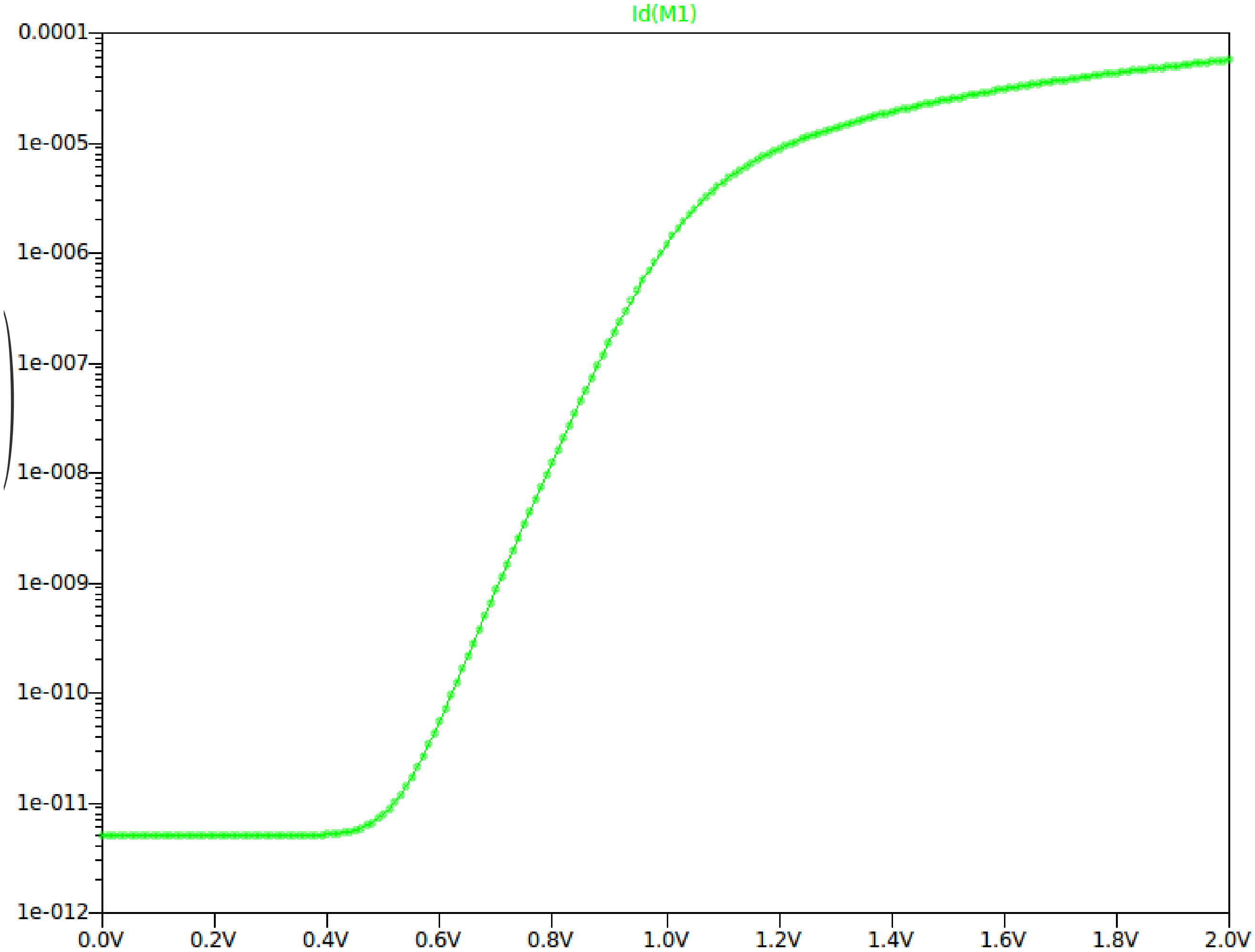
S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

Sub-Threshold I_D *vs* V_{GS}

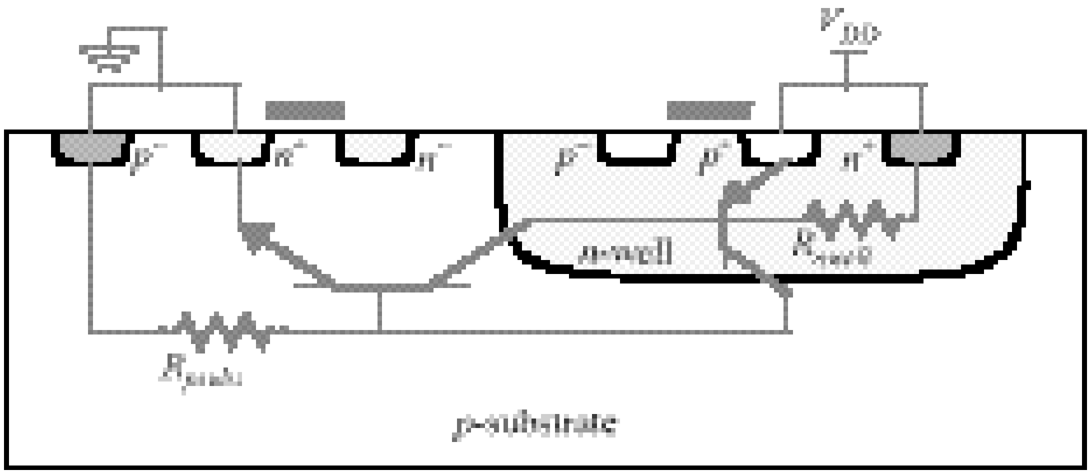
$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



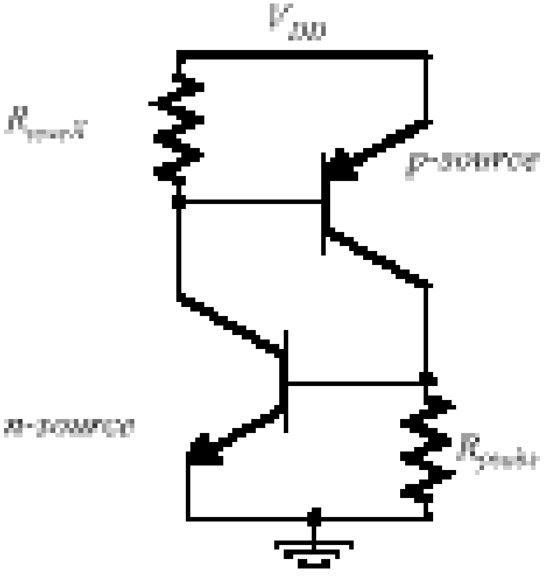
Summary of MOSFET Operating Regions

- Strong Inversion $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence

Latch-up



(a) Origin of latchup



(b) Equivalent circuit

Proceso ON semi C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.77	-0.89	volts
SHORT	20.0/0.6			
Idss		482	-274	uA/um
Vth		0.65	-0.87	volts
Vpt		13.0	-11.7	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.67	-0.94	volts
Vjbkd		10.9	-11.8	volts
Ijlk		102.5	<50.0	pA
Gamma		0.49	0.56	V^0.5
K' (Uo*Cox/2)		58.4	-19.0	uA/V^2
Low-field Mobility		476.93	155.17	cm^2/V*s

Proceso ON semi C5

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.1	104.1	23.2	1103	41.8	0.09	0.09	ohms/sq
Contact Resistance	58.9	145.5	16.0		26.7		0.89	ohms
Gate Oxide Thickness	141							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	807	801	ohms/sq
Contact Resistance	0.96			ohms

COMMENTS: N\POLY is N-well under polysilicon.

Proceso ON semi C5

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	415	721	84		28	12	7	92	aF/um^2
Area (N+active)			2453		36	16	11		aF/um^2
Area (P+active)			2357						aF/um^2
Area (poly)				869	60	15	9		aF/um^2
Area (poly2)					57				aF/um^2
Area (metal1)						30	12		aF/um^2
Area (metal2)							28		aF/um^2
Fringe (substrate)	356	227			54	33	26		aF/um
Fringe (poly)					67	37	27		aF/um
Fringe (metal1)						52	32		aF/um
Fringe (metal2)							53		aF/um
Overlap (N+active)			182						aF/um
Overlap (P+active)			234						aF/um